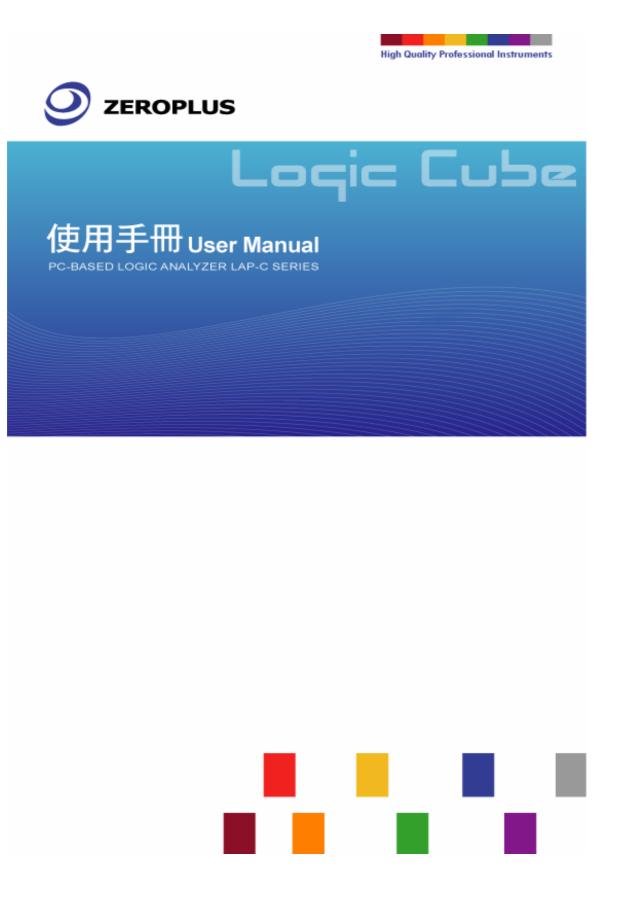


The Zeroplus Logic Analyzer User's Manual V3.12.02





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Preface

This Quick Start Guide is designed to help new and intermediate users navigate and perform common tasks with the Zeroplus Logic Analyzer. Despite its simple packaging and interface, the Logic Analyzer is a sophisticated measurement and analysis tool. It is also a highly sensitive electrical current sensing device. Users must carefully read instructions and procedures pertaining to installation and operation. Any instrument connected to the unit should be properly grounded. A pair of anti-static gloves is strongly recommended when performing a task with the device. To ensure accuracy and consistency of output data, use of the bundled components is strongly recommended.

Users' opinions are very important to Zeroplus. Please contact our engineering team by telephone, fax or email with your questions or feedback. Thank you for choosing the Zeroplus Logic Analyzer.

Notice: We will not have additional notice for you when there is any modification to the User Manual. If there is any unconformity caused by software upgrade, users should take the software as the standard.



1 Features of Zeroplus Logic Analyzer

- 1.1 Package Contents
- 1.2 Introduction
- 1.3 Hardware Specifications
- 1.4 System Requirements
- 1.5 Device Maintenance and Safety



Objective

In this chapter, users will learn about the package contents, description, hardware specifications, system requirements and safety issues of the Zeroplus Logic Analyzer. Although this chapter is purely informative, we highly recommend reading this carefully to ensure safety and accuracy when performing any operation with the Zeroplus Logic Analyzer.

1.1 Package Contents

Verify the package contents before discarding packing materials. The following components should be included with your product. For assistance, please contact our nearest distributor.

Madala	LAP-	LAP-	LAP-	LAP-	LAP-	LAP-
Models	16032U	16064U	16128U	32128U-A	321000U-A	322000U-A
Logic Analyzer	1	1	1	1	1	1
16-Pin Testing Cable	0	0	0	1	1	1
8-Pin Testing Cable	2	2	2	2	2	2
Probe	2	20	20	36	36	36
USB Cable	1	1	1	1	1	1
Quick Start Guide	0	1	1	1	1	1
Driver CD**	1	1	1	1	1	1
1-Pin Testing Cable (White)	1	1	1	1	1	1
2-Pin Testing Cable (Black)	1	1	1	1	1	1

Table 1-1: Accessories List

Models	LAP-C (16032)	LAP-C (16064)	LAP-C (16128)	LAP-C (162000)	LAP-C (32128)	LAP-C (321000)	LAP-C (322000)
Logic Analyzer	1	1	1	1	1	1	1
16-Pin Testing Cable	0	0	0	0	1	1	1
8-Pin Testing Cable	2	2	2	2	2	2	2
Probe	2	20	20	20	36	36	36
USB Cable	1	1	1	1	1	1	1
Quick Start Guide	0	1	1	1	1	1	1
Driver CD**	1	1	1	1	1	1	1



1-Pin Testing Cable (White)	1	1	1	1	1	1	1
2-Pin Testing Cable (Black)	1	1	1	1	1	1	1

* This Driver CD contains multilingual software interface program as well as multilingual User Manual.

* The following are accessories of LAP-C Series, which are the same with that of LAP-A.



Fig. 1-1: Logic Analyzer

ZEROPLUS

Fig. 1-3: Probe (varied depending on models)



Fig. 1-5: Quick Start Guide

Fig. 1-7: 1-Pin External Clock Cable (White)



16-Pin x 1 8-Pin x 2 Fig. 1-2: Testing Cable



Fig. 1-4: USB Cable



Fig. 1-6: Driver CD



Fig. 1-8: 2-Pin Ground Cable (Black)



1.2 Introduction

1. Zeroplus Logic Analyzer models LAP-16032U, LAP-16064U, LAP-16128U, LAP-32128U-A, LAP-321000U-A, and LAP-322000U-A, all share the same external features as illustrated in the following figures.

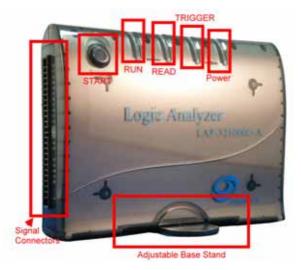


Fig. 1-9 A view of the Zeroplus Logic Analyzer LAP-A Series. See *Fig 1-12* for detailed information on the **Signal Connectors**.



Fig. 1-10 Side view of Zeroplus Logic Analyzer, which draws its power from the USB connection.

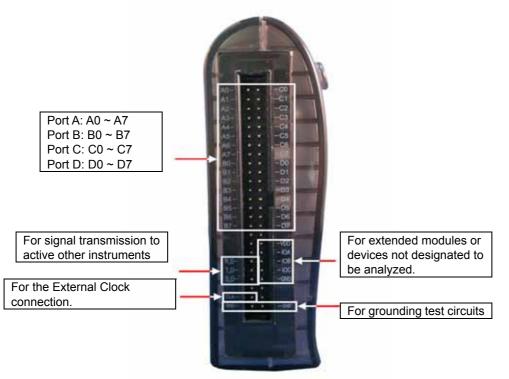


Fig. 1-11 Rear view of Zeroplus Logic Analyzer LAP-A Series



2. Zeroplus Logic Analyzer LAP-C Series share the same external features as illustrated in the following figures.



Fig. 1-12: A View of the Zeroplus Logic Analyzer LAP-C Series. See Fig 1-11 for detailed information on the **Signal Connectors**



Fig. 1-13: Side View of the Zeroplus Logic Analyzer; the power of the Logic Analyzer is drawn from the USB connection.

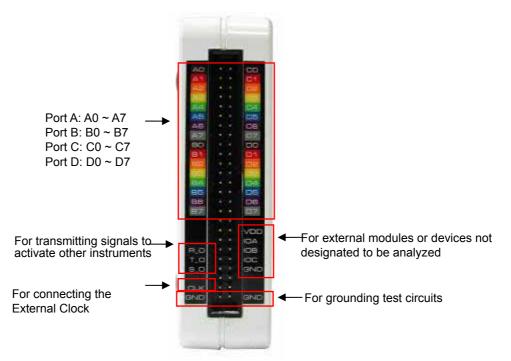


Fig. 1.14 Side View of the Zeroplus Logic Analyzer LAP-C Series



Table 1-2A: List of Functional Pins in Each Model

Models	LAP- 16032U	LAP- 16064U	LAP- 16128U	LAP- 32128U-A	LAP- 32100U-A	LAP- 322000U-A	
Port A (A0~A7)	\checkmark		\checkmark	V			
Port B (B0~B7)	\checkmark		\checkmark	V			
Port C (C0~C7)	X		\checkmark	V			
Port D (D0~D7)	Х		\checkmark	\checkmark			
R_O	\checkmark		\checkmark	\checkmark			
T_0	√		\checkmark	\checkmark			
S_0	\checkmark		\checkmark	√			
CLK	\checkmark		\checkmark	√			
GND		\checkmark		\checkmark	\checkmark		

Table 1-2B: List of Functional Pins in Each Model

Models	LAP-C (16032)	LAP-C (16064)	LAP-C (16128)	LAP-C (162000)	LAP-C (32128)	LAP-C (321000)	LAP-C (322000)
Port A							N
(A0~A7)			v		N		v
Port B			\checkmark				N
(B0~B7)			•		v		v
Port C			Х				
(C0~C7)		^			Y		•
Port D		Х				\checkmark	
(D0~D7)		*			,	,	
R_O		\checkmark			\checkmark		\checkmark
T_O		\checkmark			\checkmark		\checkmark
S_0		\checkmark			\checkmark		\checkmark
CLK		\checkmark			\checkmark		\checkmark
GND			\checkmark		\checkmark		\checkmark
VDD		\checkmark			\checkmark		\checkmark
IOA	\checkmark				\checkmark		
IOB	\checkmark			\checkmark			
IOC		\checkmark			\checkmark		
GND					\checkmark		

Table1-3: Definitions and Functions of Pins for All Models

CLK	Clock	Connect a given external module to be analyzed.
GND	Ground	Two pins used for grounding the Logic Analyzer with a given external module to be analyzed.

Table1-4: Definitions and Functions of Pins for Advanced Models (1)

R_O	Read (Out)	When the Logic Analyzer is about to upload data from the memory to the PC, the R_O will send a Rising Edge signal of DC3.3V. When the upload is finished, a Falling Edge signal is sent.
T_0	Trigger (Out)	When a trigger condition is established, the T_O will send a Rising Edge signal of DC3.3V. When the memory is full, a Falling Edge signal is sent.
S_0	Start (Out)	When a user initiates a sampling task by clicking the RUN icon in the window or clicking the START button on the device, the S_O will send a Rising Edge signal of DC3.3V.



	When the Logic Analyzer finishes uploading, a Falling Edge
	signal is sent.

Table1-5: Definitions and Functions of Pins for Advanced Models (2)

VDD	Voltage Drain (Semiconductor)	Provide +3.3 V for external modules by draining voltage from the Logic Analyzer.
ΙΟΑ	Ext. I/O Module A	Transmit signals between an external model or device and the Logic Analyzer.
IOB	Ext. I/O Module B	Same as IOA.
IOC	Ext. I/O Module C	Same as IOA .
GND	Ground	Ground external devices in sequence.



1.3 Hardware Specifications

Table 1-6A: Hardware Specifications of LAP-A Series

Items	\Туре	LAP- 16032U	LAP- 16064U	LAP- 16128U	LAP- 32128U-A	LAP- 321000U-A	LAP-322000U-A		
Inte	rface	USB 2.0 (1.1)							
Operatin	g System	Windows 2000/ Windows XP/ Windows Vista/ Windows 7							
Power	Supply	USB 1.1 (USB 2.0 Recommended)							
Chai	nnels		16			32			
	Internal Clock Rate (asynchronous)	100Hz ~	100MHz		10	00Hz ~ 200MHz			
Sampling Rate	Max External Clock (synchronous)	Max 7	'5MHz			Max 100MHz			
	Bandwidth				75MHz				
	Memory	512K Bits	1M Bits	4M Bits	4M Bits	32M Bits	64M Bits		
Memory	Memory Depth (Per Channel)	32K Bits	64K Bits	128K Bits	128K Bits	1M Bits	2M Bits		
	Trigger Channel	1	6 Channels	5		32 Channe	els		
	Trigger Condition				Pattern/Edg	ttern/Edge			
Trigger	Pre-Trigger/ Post-Trigger				Yes				
	Trigger Level		1 Level						
	Trigger Count				1~65535				
Threshold	Working Voltage				-6V~+6V				
Voltage	Accuracy				±0.1V				
	I2C				Free				
	UART				Free				
Protocol	SPI				Free				
Analyzer	1-WIRE				Free				
(Кеер	CAN 2.0B				Free				
Increasing)	HDQ		Op	otion			Free		
	7-SEGMEN T LED		Free						
	Operating Interface Language			Chinese	e(Si)/ Chinese	(Tr)/ English			
	Time Base Range				5ps~10Ms				
Software	Vertical Sizing				1~5.5				
Function	Compression	Max 8Mbits	Max 16Mbits	Max 32Mbits	Max 32Mbits	Max 255Mbits	Max 512Mbits		



	Waveform Width Display	Yes								
	Trigger Page		1~8192Page							
	Pulse Width Trigger									
	Double Mode				Yes					
	Trigger Mark			Free						
	Latch Function	Option	Option	Option	Option	Free	Free			
	Data Contrast	Option	Option	Option	Option	Free	Free			
	Multi-stacked Logic Analyzer Settings	No	No	No	Yes	Yes	Yes			
	Protocol Analyzer Trigger		Option							
Safety Cer		FCC/CE/WEEE/RoHS								

Table 1-6B: Hardware Specifications of LAP-C Series

ltems	с\Туре	LAP-C (16032)	LAP-C (16064)	LAP-C (16128)	LAP-C (162000)	LAP-C LAP-C LAP-C (32128) (321000) (322000				
Inte	rface				USB 2.0 (1.)				
Operatin	g System		Windows	s 2000/ Winc	lows XP/ Wir	ndows Vista/	Windows 7			
Power	Supply			USB 1.1	(USB 2.0 Re	commended)			
Cha	nnels			16			32			
	Internal Clock Rate (asynchronous)	100Hz ~	100MHz	100Hz ~ 200MHz						
Sampling Rate	Max External Clock (synchronous)	Max 7	Max 75MHz		Max 75MHz Max 100MHz					
	Bandwidth				75MHz					
	Memory	512K Bits	1M Bits	4M Bits	64M Bits	4M Bits	32M Bits	64M Bits		
Memory	Memory Depth (Per Channel)	32K Bits	64K Bits	128K Bits	2M Bits	128K Bits	1M Bits	2M Bits		
	Trigger Channel	16 Channels					32 Channels	;		
	Trigger Condition				Pattern/Edg	je				
Trigger	Pre-Trigger/ Post-Trigger				Yes					
	Trigger Level				1 Level					
	Trigger Count				1~65535					
Threshold	Working Voltage				-6V~+6V					



Voltage	Accuracy				±0.1V					
	I2C				Free					
	UART				Free					
Protocol	SPI				Free					
Analyzer	1-WIRE				Free					
(Keep	CAN 2.0B				Free					
Increasing)	HDQ			Option			Fre	e		
	7-SEGMEN T LED				Free					
	Operating Interface Language			Chinese	e(Si)/ Chinese	e(Tr)/ Englis	h			
	Time Base Range		5ps~10Ms							
	Vertical Sizing									
	Compression	Max 8Mbits	Max 16Mbits	Max 32Mbits	Max 512Mbits	Max 32Mbits	Max 255Mbits	Max 512Mbits		
	Waveform Width Display	Yes								
	Trigger Page				1~8192Pag	je				
	Pulse Width Trigger	Free								
Software	Double Mode	No				Yes				
Function	Trigger Mark		Option		Free		otion	Free		
	Latch Function		Option		Free	Option	Fre	e		
	Data Contrast		Option		Free	Option	Fre	e		
	Multi-stacked Logic Analyzer Settings		1	No	Yes					
	Protocol Analyzer Trigger		_	0	ption	Free				
Safety Certification		FCC/CE/WEEE/RoHS								



1.4 System Requirements

This section discusses basic operating system and hardware requirements for the Logic Analyzer. Software and hardware capability may vary along with PC configuration. This manual assumes that one of supported operating systems(listed below) is properly installed.

1.4.1 Operating System Requirements

	Support	Non-support
Operating System Name	 Windows 2000 (Professional, Server Family) Windows XP (Home, Professional Editions 32-Bit version) Windows VISTA (32-Bit and 64-Bit version) Windows 7 (32-Bit and 64-Bit version) 	 Windows NT 4.0 (Workstation & Server, Service Pack 6) Windows Server 2003

1.4.2 Hardware System Requirements

Hardware Name	Lowest Configuration	Recommended Configuration
CPU	166 MHz	900 MHz
Memory	64MB	256MB
Display Device	VGA Display Capability with 1024x768 resolution or higher.	VGA Display Capability with 1024x768 resolution or higher.
Hard Drive	At least 100MB available space	At least 100MB available space
USB	USB1.1 supported	USB2.0 recommended



1.5 Device Maintenance and Safety

Follow these instructions for proper operation and storage of the Logic Analyzer.

Table1-7: General Advice

Cautions	 Do not place heavy objects on the Zeroplus Logic Analyzer. Avoid hard impacts and rough handling. Protect the Logic Analyzer from static discharge. Do not disassemble the Zeroplus Logic Analyzer; this will void the warranty and could affect its operation.
Cleaning	 Use a soft, damp cloth with a mild detergent to clean. Do not spray any liquid on the Zeroplus Logic Analyzer or immerse it in any liquid. Do not use harsh chemicals or cleaners containing substances such as benzene, toluene, xylene or acetone.

Table1-8: Electrical Specifications(LAP-A Series & LAP-C Series)

Items	Minimum	Typical	Maximum
Working Voltage	DC 4.5 V	DC 5.0 V	DC 5.5 V
Current at Rest			200 mA
Current at Work			400 mA
Power at Rest			1 W
Power at Work			2W
Error in Phase Off*			1.5 nS
V _{input} of Testing Channel	DC -30V		DC 30 V
V _{Reference}	DC -6V		DC 6 V
Input Resistance		500K /10pF	
Working Temperature	5°C		70°C
Storage Temperature	-40°C		80°C

* Refer to the User Manual for error analysis calculation.



Table1-9: Operating Environment

WARNING	 Avoid direct sunlight Use in a dust free, non-conductive environment (see Note) Relative Humidity: < 80% Altitude: < 2000m Temperature: 0 ~ 40 Degrees C This is a Class A product which may cause radio interference in a domestic environment. Note: EN 61010-1:2001 specify degrees of pollution and their requirements. Logic Analyzer falls under Level 2. Pollution refers to 'addition of foreign matter, solid, liquid or gaseous (ionized gases), which may produce a reduction of dielectric strength or surface resistivity'. Pollution Degree 1: No pollution or only dry, non-conductive pollution occurs. This pollution has no effect. Pollution Degree 2: Normally only non-conductive pollution occurs. Occasionally, however, temporary conductivity caused by the condensation must be expected. Pollution Degree 3: Conductive pollution occurs or dry, non-conductive pollution which becomes conductive due to the condensation occurs. In such conditions, the equipment is normally protected against exposure to direct sunlight, precipitation and wind, but neither temperature nor humidity is controlled.
Storage	Relative Humidity: < 80%
Environment	Temperature: 0 ~ 50 Degrees C

Conclusion

After reading this section, users should have a basic grasp of the Logic Analyzer. A complete understanding of the section, **Device Maintenance and Safety**, is a critical prerequisite of any further operation as presented in the User Manual.



2 Installation

- 2.1 Software Installation
- 2.2 Hardware Installation
- 2.3 Tips and Advice



Objective

This chapter describes the installation of the Logic Analyzer hardware and software. Software installation steps must be followed precisely to ensure successful installation.

2.1 Software Installation

In this section, users will learn how to install the software and drivers. As with proper installation of many USB devices, the Logic Analyzer application and driver software must be installed prior to the connection of the hardware. The following steps illustrate an installation of a Zeroplus **LAP-C V3.12** Logic Analyzer. The other twelve models mentioned in Chapter 1 would follow identical procedures.

Step 1. Insert the driver CD-ROM in the PC CD drive.

Step 2. Execute the installation program. Go to the START menu, click **START**, **Run**, **Browse** in sequence, select **Setup.exe** file in the appropriate model folder and then click **OK**. It is recommended that all other programs are closed while the installation proceeds.

Step 3. Choose the Application Setup.

Step 4. Click Next to proceed with the Install Wizard.

Step 5. Select "I accept the terms of the license agreement", and click Next.

Step 6. Enter User and Company names.

Step 7. Choose the setup type. We recommend Complete for most users.

Step 8. Click Install to confirm settings and begin the actual installation.

Step 9. Click Finish to complete the installation.

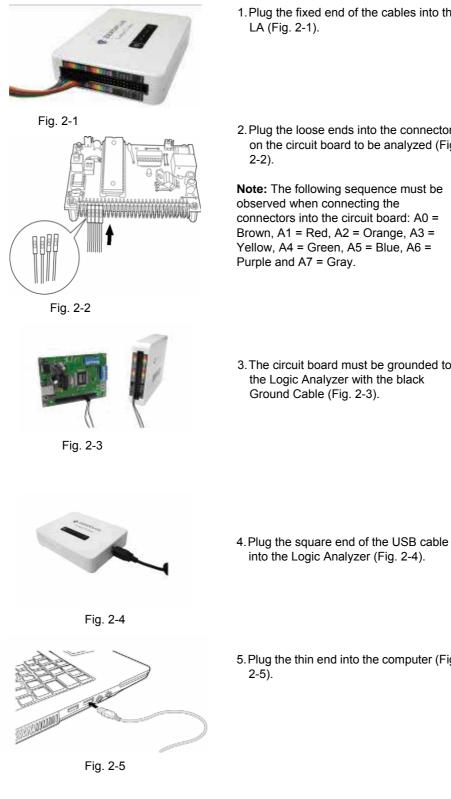






Hardware Installation 2.2

Hardware installation simply involves in connecting the Logic Analyzer to your computer with the included USB Cable as shown in Figures 2-4 and 2-5.



1. Plug the fixed end of the cables into the

2. Plug the loose ends into the connectors on the circuit board to be analyzed (Fig.

Note: The following sequence must be observed when connecting the connectors into the circuit board: A0 = Brown, A1 = Red, A2 = Orange, A3 = Yellow, A4 = Green, A5 = Blue, A6 =

3. The circuit board must be grounded to the Logic Analyzer with the black Ground Cable (Fig. 2-3).

5. Plug the thin end into the computer (Fig.



At this point, the computer should be able to detect the Logic Analyzer and finalize the installation for hardware connection. For further information, refer to the Troubleshooting and Frequently Asked Questions (FAQ) chapters in the User Manual.



Fig. 2-6: An Assembly of Laptop, Logic Analyzer and Testing Board of LAP-C Series

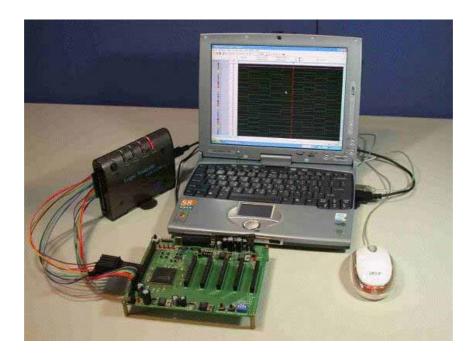
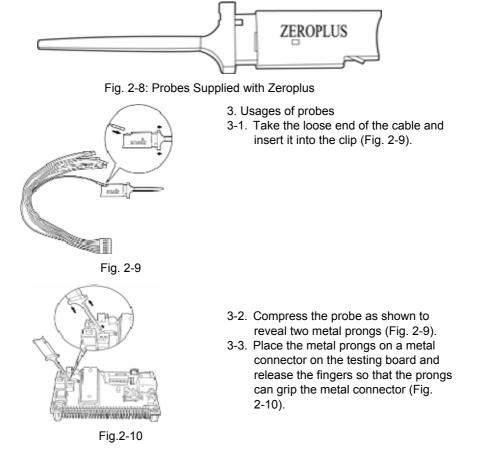


Fig.2-7 An Assembly of Laptop, Logic Analyzer and Testing Board of LAP-A Series



2.3 Tips and Advice

- 1. When testing a circuit board, make sure that the internal sampling frequency (within the Logic Analyzer) is at least four times higher than the external board frequency.
- 2. If the signal connector does not work well with the pins on the test board, try to use the supplied probes.



- 4. The Logic Analyzer will connect to the **Zeroplus** server for software updating automatically if internet is available.
- 5. Unwanted signals can be filtered out by using the **Signal Filter** or **Filter Delay** function.
- 6. During long-time measuring, **Compression** would make memory work more efficient.
- 7. Trigger condition depends on the testing board. If triggering does not work well, try to narrow the trigger conditions and optimize them repeatedly.
- 8. If testing board's frequency is lower than that of Logic Analyzer, users shall sample signals according to the external clock.
- 9. When external clock is used for sampling, users could filter extra signals with the Signal Filter function.
- 10. Unused channels could be removed from the Bus/Signal column in the dialog box of Channels Setup(on the popup menu of Bus/Signal column).



3 User Interface

- 3.1 Menu & Tool Bars
- 3.2 Find Data Value
- 3.3 Statistics Feature
- 3.4 Customize Interface
- 3.5 Auto Save
- 3.6 Color Setting
- 3.7 The Flow of Software Operation



Objective

Chapter 3 presents detailed information on the Logic Analyzer software interface in four sections: **Menu Bar**, **Tool Bar**, **Statistical Function**, and **Interface Customization**.

Basic Layout

The layout of the Logic Analyzer software interface can be divided into nine sections as shown in the following figure.

II II 4	00	and the second second	03240us • 🗶 🕱	2 2	LLLF	1+ et (and the second	Height Pa	And and a second se	ger Delay	18us
at 20 Altma		Disata	B 108-747 406103	is_ <u>B</u> F	bs 150us *		B-Tell	õus -	ĉ	Stripe Plate No	
Burlight	1 igger	Film	16	-15	4	16	à	5 1	0 15	25	\geq
🖌 AQ 🚐	- 26	1.92	10101010101010	10 10 10	10 10 10 10	10 10 10 10	10 10 10 10	10 10 10 10	10 10 10 10	10 10 10 10	10 10 10
# AL /II	- 22 -	1	0 20us 20us 2	0us 20us	20us 20us	2015 2013	20us 20us	20ut 20ut	20us 20us	20us 20us	20ut 20
# A2, 53	- 32	1.35	40 40us	40us	40us	40us	40us	40us	40us	40us	40us
6 A3 - 61	- 26	- 34	30 80ut		80	15	80	ius .	80	lus	
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# 47 22	- 28	35						27ms			
¥ 10.11	0	26 .				0		7.2ms			
-5	6	7.	[8		7.2ms			
₩ 82_1111	一招	12						9.2ms			
< 10 H	- 22	X						9 2ms			
6 34 35	18	K						2ms			
# 05 100	- 36	36						9.2ms			
# 56 III.	- 26	8						9.2ms			
# 10 ST	- 22	35						2/118			
#α =	- 26	R.						3.2ms			
CI CI	- 52	30						7.2ms			
€ G G	35	36						1.2ms			
a a	26	. 30						3.2ms			
# 64 CA	38	10.00						8.2mi			/

1. Menu Bar

All operations are performed directly from the menu bar, including **configure label**, **rename**, **execute** and **stop**. Pull-down menus allow easy navigation through the measurement panel.

2. Tool Bar

The tool bar is the graphical user interface which can make you work with some of the more common applications. From these icons, you can change settings and operate the Logic Analyzer easily.

Note: The prompting information of the shortcut keys has been added in the tooltips of the Tool Bar, that is to say, when users place the cursor on the icons, the corresponding shortcut key information will appear. For example, the prompting information of the New button is "New (Ctrl+N)". "Ctrl+N" is the Shortcut Key of the function of New.

3. Information Bar

The Information Bar displays information about the grids in the waveform, such as: Address, Time, Frequency, Trigger Bar, A Bar, B Bar and other Bar. Details of the labels are below:

- Scale Define the acquisition clock that controls the data sampling
- Total The period of time when Logic Analyzer captures data.

Display Pos - The middle tip means the middle position of the waveform.

Display Range-Display the waveform time range of the current waveform display

- area.
 - A Pos The main function is to set A Bar or the other Bar.
 - B Pos The main function is to set B Bar or the other Bar.
 - A-B Press the under arrow to exchange and become the other Bar

Moreover, you also can execute this function from the other Bar.

4. Ruler (Waveform Display / Listing Display)

Ruler shows the time position of the waveform shown in the waveform display area or the listing display area.



5. Bus/Signal (Waveform Display / Listing Display)

Edit names of the measured channels; color shown matches the trace color.

6. Trigger Column

Trigger Column allows users to adjust signal trigger conditions.

7. Filter Column

Filter Column allows users to set Bus or signal filter conditions.

8. Display Area

Acquired data is displayed as a waveform or in a list format.

Waveform Display

This interface shows the digital signals. When the signal is logic "0", the waveform will be displayed as _____. If the signal is logic "1", the waveform is as _____. An unknown signal waveform is displayed in gray between the high and low levels as _____. There are sixteen channels in LAP-16032U, LAP-16064U, LAP-16128U, LAP-C(16032), LAP-C(16064), LAP-C(16128) and LAP-C(162000), and thirty two channels in LAP-32128U-A, LAP-321000U-A, LAP-322000U-A, LAP-C(32128), LAP-C(321000) and LAP-C(322000).

Listing Display

This interface shows the digital signals as 1 and 0. Logic 1 is displayed as "1" and logic 0 is displayed as "0".

9. Status Area

Display Logic Analyzer status. The function name is also indicated here.



3.1 Menu & Tool Bars

Section 3.1 presents detailed information on the eight menu and thirteen tool items shown in the menu bar. The eight menu items are **File**, **Bus/Signal**, **Trigger**, **Run/Stop**, **Data**, **Tools**, **Window** and **Help**. The thirteen tool items are **Standard**, **Trigger**, **Run/Stop**, **Sampling**, **Trigger Content Set**, **Display Mode**, **Windows**, **Mouse Pattern**, **Zoom**, **Data**, **Show Time/Height**, **Trigger Delay** and **Font Size**.

1. File



Fig 3-2: File menu.

- ← Close Close the file being worked on.
- ← Auto Save-Save the required file automatically.(See Section 3.5 for detailed instructions)
- Export Waveform-Export files into Text (*.txt) and CSV Files (*.csv)
- Export Packet List Export the active packet list.
- ← Language Allow users to change the language interface of menus, tool boxes, etc.
- ← Print Preview Show three options: Bus/Signal & Trigger & Filter, Position Display Area and Waveform Display Area (See Fig. 3-17).
- ← Exit Exit the program.



Fig 3-3: File Tool Box



Menu Bar: File

Menu Item		Detail Menu & Dialog Box
New	Ctrl+N	Open a New file.
ເ∕r Open	Ctrl+0	Look, jr In10044.4AP-80M W Floor Fle game: W Floor In10044.4AP-80M W Floor Fle game: W Fleorer In10044.4AP-80M Fleorer In10044.4AP-80M W Fleorer Fleogram W Fleorer Fleogram Fleorer Fleorer W Fleorer Fleorer Wodde No: Note

Fig 3-4: Open an existing file.

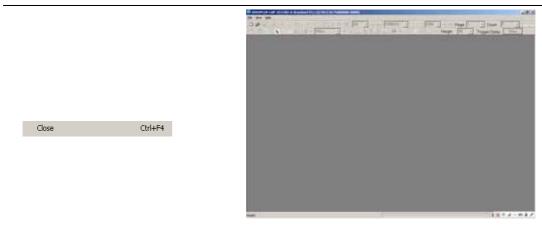


Fig 3-5: Close the active workspace.

	Save As	1×
	Savejiz 🗀 811004LAP-80M 💿 🔶 🗈 🖆 🖬-	
Save Ctrl+S Save As Auto Save	Wy Fladerit Wy Fladerit Desktop My Documents Wy Computer My Nichrosk: Places	ave
		<u> </u>
	Fig 3-6: Save As Dialog Box	



🏧 Export Waveform...

Ctrl+Shift+E

Save As - Specify the name of the file to be saved. Auto Save - Save the required file automatically.

laport Tavefo									<u>1</u> ×
保存在 ①:	V3.12				٣	\leftarrow	S (1	•	
記念 記念 記念 記念 記念 記念 記念 記念 記念 記念	OFT Szeropl Szeropl	uz_la_nes	n_ni						
	文件名 @ 保存类型(tat ezt Filer	(*. txt)			×		保存(5) 取消
Bus Output Para	meter D	ata Inform	uation						
@ Yes C I	No (ata Style	ALL			٣	Bus R	sticset))
Perform Model		ata Model	Al De	ta		v			
	(Data Forma	e Hexa	decimal		۲			
Output Range									
From Beginn	ing of Data	-10.3	23ms	To E	nd of Data		• 10	.25ms	
The allowable n	nax number (of lines of	each expo	ted file (10	00~60000)	6000	0		
Pop up an exp									

Fig 3-7: Export Waveform Dialog Box

Export Waveform: Export a file into text (*.txt) or CSV (*.csv) formats. Bus Output Parameter: Decide whether or not to display the parameters of the file to be exported.

Perform Model: Choose whether to export the data either vertical or horizontal.

Data Style: Include ALL, ALL BUS, PROTOCOL (HAS CHANNELS), PROTOCOL(NO CHANNELS).

Data Model: Export data changed function; the selected items inc lude ALL Data, Sampling Changed Dot (Compression), Data Cha nged Dot (Compression). Some of the data value for the signal c hannels of sampling position are the same, for example, view the data changed and decrease export capacity; this function will be good for users.

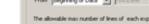
Output Range: Choose the range of the data to export from the pull-down menus.

The allowable max number of lines of each exported file (1000-60000): After activated, users can self-define the display row number of exported file (1000-60000)

Pop up an export file automatically: The export file can be popped up automatically. Users can decide whether to activate the function; the default is selected. See the export file below:

A UK speed op one Therein for using /CEOPTIST large Analytee Version VI.1 Version VI.1	11.0	-						_					1.01	1.0
Thanks for using (2000/PLS) Logic Adulates Version V211 (Incomme 111:0) (Incomm	1.24	figned the st	_	0110121	NAME AND ADDRESS			1.7.01.77	1000					15
View scale 10 48 File straded on: 2011/07/24 Logic Avoinger Setting information Sequences when you want in the strategy of					ninig 2010 Venia	P(153.00	c Analyzee							100
Logic Anosters integri effective Logic Anosters integri effective Steering and Strandard Steering and Strandard Steering and Strandard The problem integritery and the steering and strandard st			i.											
Signal Effets using: Table Conditions lengthere a structures: no Decky lines (Double) (Th' Stands he the signal of high patters), 'LL' presents the signal of two patters and 'LL' means here' care. Signal Tragge structure, Data (Th' Stands he the signal of high patters), 'LL' presents the signal of two patters and 'LL' means here' care. Signal Tragge structure, Data (Th' Marcin Research (Stand), 'LL' presents high patters and 'LL' means here patters. The signal register structure, Data (The signal of mersuper total), of DAT, Accordeng The Conducts or of the organized fits to present. The signal of mersuper total, of DAT, Accordeng The Conducts or of the organized fits to present. The signal of mersuper total, of DAT, Accordeng The Conducts or of the organized fits to present. Sole (DAS) The signal of mersuper total, of DAT, Accordeng The Conducts or of the organized fits to present. Sole (DAS) The signal of mersuper total, of DAT, Accordeng The Conducts or of the organized fits to present. Sole (DAS) The signal of mersuper total of DAT, Accordeng The Conducts or Other organized fits to present. Sole (DAS) The signal of mersuper total of DAT, Accordeng The Conducts or Other organized fits to present. Sole (DAS) Sole (DAS) Sole (DAS) Sole (DAS) Sole (DAS) Sole (DAS) Sole (DAS) Sole (DAS) Sole (DAS) So	Logi Sarq Roter Roter The The Trip	e Analyster pling mode real cample l'use = 218 e dise Data mutidier of reinder of ger Propert Tay big	setup info standard ng freigue Compress Rus – 0 Channat- tes Trop ger ficset ger chan	normations mary = 100 norm = 12 per position t = 1 t = 1	on - 50%		e – 1.50 v	it n	et = 1.30¥	10 %	e = 1.549	2		
1 84 85 86 87 E0 C1 C2 E1 C4 E5 C6 E2	Sign CHI Tops The	ul l'éter set Diviay l "stands hor al Tropper s display and display of r	top Filter time: Divi Oter sages enflag: (1 W,1 metal) thopgen s metalogi	er Condition all of heigh Di," stands vs. Rosing E setsgi of de Tintalt, 20.	gutteren, 1 Nor doert Lolge, 1917 Ner Accord Littere	"L1" prese care. "The presents long the c0 Scale.	sits the say "presents Falling Edg tacacter of t 10x5	heigh gudb e. 1781° 6	een and 1%	1" minutes Effect.				
	(Char							45	- 46	12	**		12	

Fig 3-8: Export File





Report Packet List 7 ×						
保存在 (1): 😼 我的电脑						
文件名 (6): (現存 (3)) (保存委型 (1): Text Files(#.txt) 王 取消						
Bus Output Parameter Data Format Export Format © Ytts No Hexadecimal Iteration						
Output Range From First Packet						
P Pop up an export file automatically						

Fig 3-9: Export Packet List Dialog Box

Users can use paperwork, register and analyze packet list data.

The allowable max number of packets of each exported file (1000-5000): After activated, users can self-define the display packet number of exported file (1000-5000).

Pop up an export file automatically: The function of popping up an export file automatically in the Export Packet List dialog box is the same with that of the Export Waveform dialog box.

Export Format: The Export Format is convenient for users to use the captured data in the following process. There are two formats for selecting, Report Form and Pure Data Form. See the following picture:

Bus Output Parameter	Data Format	Export Format Pure Data Form Report Form	Option
Output Range		Pure Data Form	
From First P	acket 💌	To Final Packet 💌	
1		5	

Fig 3-10: Export Format Pull-down Menu

In the part of the Export Format, when the users select the Report Form, the "Option" button can't be used; when users select the Pure Data Form, the "Option" button can be used. The "Option" pops up the Option dialog box as follows, where users can customize the export data items in the dialog box which are Packet #, Name, TimeStamp, Length and DESCRIBE.

Option	×
Options	
🔽 Packet#	🗹 Length
✓ Name	
🔽 TimeStamp	
	OK Cancel

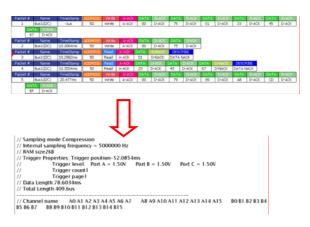
🙋 Export Packet List...

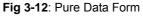


Fig 3-11: Option Dialog Box

For instance, all the export options are selected entirely. See the below

picture:





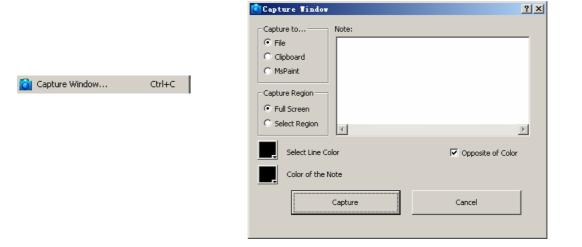


Fig 3-13: Capture Window

This feature is equivalent to [Alt]+[Print Screen], or [Print Screen]

Capture to

File – Save the captured image as either a jpeg or bmp Clipboard – Copy the captured image to the clipboard for use in other applications.

MsPaint - Directly start MsPaint to view the captured image.

Capture Region

Full Screen – Capture everything on the screen.

Select Region – After pressing the capture button, a cross-hair will appear on the screen. Left click the mouse button to drag an area to capture.

Select Line Color – Click the color box to change the color.

Opposite of Color – Click this check box to ensure that the note text will be the opposite of the line color.

Color of the Note- Choose the color of the note text.

Note – Type in a note to attach to the captured image.

Capture – Click the button to capture the image.



Language

Cancel - Click Cancel to end the capture.

	China and City
	Chinese(Si)
	Chinese(Tr)
•	English

Fig 3-14: Choose among Chinese Simplified (Si), Chinese Traditional (Tr) and English.

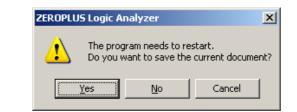
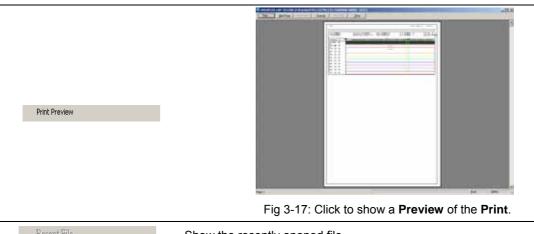


Fig 3-15: When changing languages, the above screen will be displayed and the program will need to be restarted.

	Print	? ×
Print Ctrl+P	Name: NLUPY_CNVbp Lases/et 1000 Properties	
Tip:	Status: Ready Type: hp Laseu/et 1000 Where: USB001	
This function has been	Connent:	
enhanced; now users can	Print range Copies Copies Number of gopies: 1 1	
select the pages which they	C Pages (non 1 jo 272	18
want to print or only the	C Current Page	
Current Page.	OK Cancel]

Fig 3-16: Click to enter the Print dialog box.



Recent File	Show the recently opened file.
Exit	Exit the program.



2. Bus/Signal

III, Sampling III, Channel III, Signal Fi	s Setuj	p				2	Clock Source	
Group in Ungroup				Ctrl+			Internal Clo Frequency	
Expand Collapse Format					,	A	Synchronous Cl	ock
Rename							love Left/Up love Right/Down	-dge dge ternal clock v
Port	_			1.01	dd		ide how All	
Tr.Condition	X	X	X	X	X	c	olor	
Fi.Condition	X	X	X	X	X	X	RAM Size: 2k	-
A0	7	6	5	4	3	2	Channel numbe	r will be
A1	7	6	5	4	3	2	limited to 32	

Fig 3-18: Bus/Signal Menu.

	🐢 🐺 📲 🔟 🕨	• 🕪 🔲 2K	▼ 🕷 🐝 🚺 5MHz	🔻 🗤 🛲 50% 💌 🎋 🐳
--	-----------	----------	--------------	-----------------

Fig 3-19: Trigger Tool Box.



Menu Bar: Bus/Signal Menu Item **Detail Menu & Dialog Box** Sampling Setup x Clock Source Asynchronous Clock Internal Clock Frequency: SMHz • Synchronous Clock 🏨 Sampling Setup ... C External Clock 🙃 Rising Edge C Faling Edge (Min:0.001Hz, Max:100MHz) Note: The external clock voltage level is the same as the port A trigger level Sampling RAM Sk Compression Mode Signal Filter RAM Size: 2K • Data Compression Channel number will be limited to 24 ΟK Cancel Restore Defaults Help Fig 3-20: Sampling Setup See Section 4.1 for detailed instructions. Tip: 2K कोक 🚻 50MHz ຠຠຠຠ lcon Description Decrease **₽**II4 Fig3-21: RAM Size RAM Size Increase Choose the RAM Size and the internal clock frequency from I HI RAM Size the pull-down menus. Decrease Internal nn Clock Frequency Increase Internal រារារា Clock Frequency The amount of the acquired data that can be stored by the Logic Analyzer depends on the amount of the allocated RAM. The total depth of the memory for the LAP-A/C is 128K Bits in each probe. If the Logic Analyzer starts gathering data with a 128K memory range, it will take a long time to find the required information. RAM Size In order to avoid spending a lot of time gathering data, select a smaller RAM Size. The RAM Size options are 2K, 16K, 32K, 64K, 128K and 256K. So, if gathering data with 128K takes a long time why does 256K make sense? The reason for this extra RAM Size is to cope with the fact that a few of the 1~16 channels may have a large data input. Use the pull-down menu to choose the speed of the clock on Tip: the board being tested. **Clock Source** Asynchronous Clock The sampling frequency should be more than 4 times higher than the signal to be measured so that the waveform duty cycle depiction will be accurate.

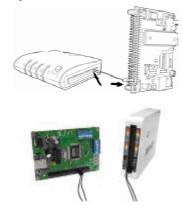
Sampling Setup

Clock Source	
Asynchronous Clo	ck
 Internal Clock 	
Frequency:	100KHz 🔽
	100Hz
Synchronous Clock	500Hz 1KHz
C External Clock	5KHz
💿 Rising Ed	25KHz
C Falling Ed	200KHz
Note: The exte	
	800KHz
	1MHz
_ Sampling	10MHz 25MHz
RAM Size	50MHz
RAM Size: 16K	80MHz
I TOK	100MHz
	150MHz 200MHz
	2001112
Apply	OK Can

孕龍科技股份有限公司

Zeroplus Technology Co., Ltd.

Synchronous Clock of LAP-A/C



Compression



Check the box to compress all the data.

Compression is used to compress acquired data through a lossless compressor. The purpose of this compression is to place more data in a limited memory than in an actual memory. The compression rate of the Logic Analyzer can be up to 255 times. This means that the maximum acquisition can be 32M Bits (128Kx255= 32M Bits) for each channel. The chosen capacity of the memory, 1MB, means that the maximum data being sieved out arrives at 1MB*255=255M Bits (Per Channel). **Note:** The rate will change depending on the data being analyzed.

Choose the frequency of the clock on the board of the Logic Analyzer. Select "External Clock" to acquire data through external sampling. Choose either "Rising Edge" or "Falling Edge" to execute the analysis process.

According to the users input the value of external frequency in software, the software can count the relevant value about signal mode and frequency. For example: the value of the message, the time scale and the zoom in and out will be the value of time mode.

Connecting the Synchronous Clock

Use one of the single connecting cables to put one end on the testing board and the other in the LA as shown in the diagram opposite.



T	p:

Signal Filter Setup

PortA	Trigger Condition	23							
		-	-		8			8	×
	Filter Condition							8	
Port®	Trigger Condition		×	X			X	8	
	Filter Condition								
PortC	Trigger Condition		120	12			10		
Ponc	Filter Condition								
PortD	Trigger Condition								
ronD	Filter Condition								
Select Filter Delay Mode C According to Filter Condition C Occosete of Filter Condition		Select Delay Start Point				Delay Tin 10us (Min: 10us	4		
play Bar Show Bar S	8ar						(Maic 655		

Fig 3-22: Signal Filter Setup Dialog Box

The function of Signal Filter is to use an alterable judgment circuit which can filter undesired signals in order to capture and store valuable data in the memory. When the combination of input signals from each channel meets the filter conditions, the section of acquired data will be gathered by the Logic Analyzer and stored in the memory. After storing the data, it will return to the Logic Analyzer's system and be displayed as a waveform. If the combination does not meet the filter conditions, it won't gather and store data.

1. **EXAMPLE** = Don't Care means that the Logic Analyzer captures all signals from sampling.

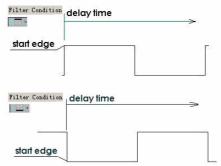


Fig 3-23: High and Low Levels

It is the system default.

2. High Level means that the Logic Analyzer captures and displays the input signals satisfying the high level.

3. **EXAMPLE** = Low Level means that the Logic Analyzer captures and displays the input signals satisfying the low level.

Tip:

Tip:

Select the Signal Filter Setup from the pull-down menu of the Bus/Signal or click the right icon or the Button on the Sampling Setup dialog box to open the Signal Filter Setup dialog box.

There are three modes of Signal Filter

configuration for each channel.

FM07I4A



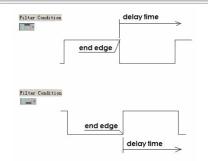


Fig 3-24: High and Low Levels

Signal Filter Delay Setup Filter Delay – According to the filter condition. Start Edge – Show the waveform from the start edge to the delay time interval.

See details in Section 4.1.

Channels Setup Tip: Channels Setup	Image: state of the state of			
Tip:	See details in Section 4.2. Click the Add Bus/Signal button to add a channel. This will appear as ' New0'.			
Add Bus/Signal	Click the Bus or channel you want to delete and press the Delete Bus/Signal button.			
Delete Bus/Signal	Press the Delete All button to delete all the Buses and channels.			
Delete All	Press Restore Defaults to return all channels and Buses t the system defaults.			
Restore Defaults	Select this function when adding and deleting channels, the software reserves the original waveform; not select this function, the waveforms in channel are cleaned up.			
Group into Bus Ctrl+G	Signals can be grouped into Buses by pressing Ctrl + G .			
Reserve waveform data and show them	Signals can be added, deleted ,copied and grouped into Bus, using the mouse or the keyboard, or right click and select the desired operations from the pull-down menu The movement of a signal channel are Auto Size (not available in waveform display), Move Left/Up, Move Right/Down, Hide, Show All and Color)			
Ungroup from Bus Ctrl+U	Ungroup signals from Buses by pressing Ctrl + U.			
Expand	A Bus contains at least 1 channel. In order to see these channels click the symbol before the Bus name. Bus/Signal Trigger Filter 000000000000000000000000000000000000			



			Fi	g 3-26: Exp	band	
		e Bus has been name to Colla			the ▼ syı	mbol before the
		▼ Bus1				XXXXXX
		• A	0 A0	\square	\square	
		• A	1 A1	\square		20 20 :
Collapse		🍼 A2 A2				40us 40u
		🧹 A3 A3				80us
		🥑 A4 A4				160us
		🥑 A5 A5				
		🍼 A6 A6		\square	\boxtimes	
			Fię	g 3-27: Coll	apse	
Formal David			Â	ito Size		
Format Row				ove Left/Up		
			M	ove Right/Do	own	
				de		
			St	iow All		
			Co	olor		
ip:		Fig 3-28: Cli	ck to c	hange the	Bus or s	ignal display.
Format Row	Cha	nge the display	of a B	us or a sigi	nal.	
Auto Size (it is not available in Waveform Display mode)	Size	the signal colu	mns a	utomatically	у.	
Move Left/Up (change to Move Left in	•	light a signal o				•
Listing Display)	•	al or Bus up (le nlight a signal or		•		•
Move Right/Down (change to Move Right in Listing Display)	-	signal or Bus do			-	
	High	nlight a signal or	Busa	and click Hi	de to hic	le it.
Hide	Clic	< to show all sig	nals a	nd Buses tl	hat have	been hidden.
Show All Color	High	nlight a signal oi	Busa	and click Co	olor to c	hange the color
Rename	•	nlight a signal or gnal.	Bus a	and click Re	ename to	o rename the B



3. Trigger

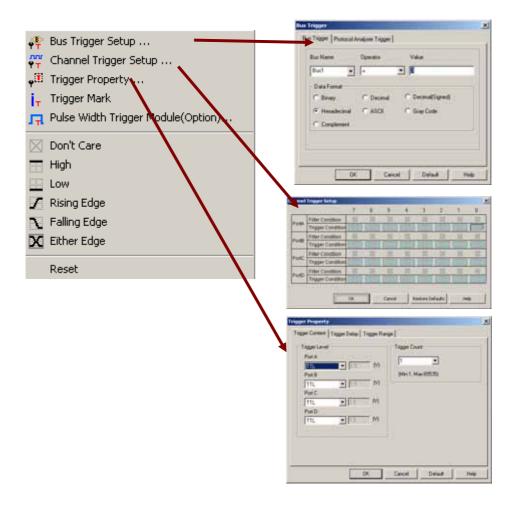


Fig 3-29: Trigger Menu



Fig 3-30: Trigger Tool Box



Menu Bar: Trigger Menu Item Detail Menu & Dialog Box Bus Trigger

	Bus Trigger	×
	Bus Trigger Protocol Analyzer Trigger	
	Bus Name Operator Value	
📲 Bus Trigger Setup	Bus1 = E	
	C Binary C Decimal C Decimal(Signed)	
	Hexadecimal O ASCII O Gray Code	
	C Complement	
	OK Cancel Default H	elp

Fig 3-31: Set Bus Trigger

See Section 4.1 for detailed instructions.

	Channel Trigger Setup					
	7 6 5 4 3 2 1 0					
	PortA Filter Condition X X X X X X X					
硸 Channel Trigger Setup	Fitter Condition					
*T	PortB Filter Condition X X X X X X X					
	Filter Condition X X X X X X X X					
	PortC Trigger Condition X X X X X X X					
	PortD Filter Condition X X X X X X X X					
	Trigger Condition					
	Cancel Restore Defaults Holp					
	Fig 3-32: The trigger action tells the Logic Analyzer when t					
	send data to the PC. The trigger conditions determine whe					
	the trigger point starts to record the information.					
📮 Trigger Mark	Open the Trigger Mark function.					
Trigger Mark	See Section 4.1 for detailed instructions.					
	Pulse Width Trigger Module: Set a trigger condition for					
📊 Pulse Width Trigger Module(Opt						
 및 Pulse Width Trigger Module(Opt Tip:	on) single channel, and the signal in this channel can t					
	on) single channel, and the signal in this channel can be triggered in the predetermined range. However, the function is required to use with the hardware of the Pulse					
Tip:	on) single channel, and the signal in this channel can the triggered in the predetermined range. However, the function is required to use with the hardware of the Pulse with the trigger Module. (If you want to learn the details)					
Tip: It is not necessary to register	on) single channel, and the signal in this channel can be triggered in the predetermined range. However, the function is required to use with the hardware of the Pulse width Trigger Module. (If you want to learn the detain please refer to the Specification of the Pulse Width Trigger Module.					
Tip: It is not necessary to register	on) single channel, and the signal in this channel can be triggered in the predetermined range. However, the function is required to use with the hardware of the Pulse width Trigger Module. (If you want to learn the detain please refer to the Specification of the Pulse Width Trigger Module.)					
Tip: It is not necessary to register can be used for free.	on) single channel, and the signal in this channel can be triggered in the predetermined range. However, the function is required to use with the hardware of the Pulse width Trigger Module. (If you want to learn the detain please refer to the Specification of the Pulse Width Trigger Module.					
Tip: It is not necessary to register	on) single channel, and the signal in this channel can be triggered in the predetermined range. However, the function is required to use with the hardware of the Pulse width Trigger Module. (If you want to learn the detain please refer to the Specification of the Pulse Width Trigger Module.)					
Tip: It is not necessary to register can be used for free.	on) single channel, and the signal in this channel can the triggered in the predetermined range. However, the function is required to use with the hardware of the Pulse Width Trigger Module. (If you want to learn the detain please refer to the Specification of the Pulse Width Trigger Module.) Set the trigger condition as " Don't Care "					
Tip: It is not necessary to register can be used for free.	on) single channel, and the signal in this channel can be triggered in the predetermined range. However, the function is required to use with the hardware of the Pulse as it width Trigger Module. (If you want to learn the detain please refer to the Specification of the Pulse Width Trigger Module.) Set the trigger condition as "Don't Care" See Section 4.1 for detailed instructions.					
Tip: It is not necessary to register can be used for free. Don't Care High	on) single channel, and the signal in this channel can be triggered in the predetermined range. However, the function is required to use with the hardware of the Pulse as it Width Trigger Module. (If you want to learn the detate please refer to the Specification of the Pulse Width Trigger Module.) Set the trigger condition as "Don't Care" Set the trigger condition as "High"					
Tip: It is not necessary to register can be used for free.	on) single channel, and the signal in this channel can the triggered in the predetermined range. However, the function is required to use with the hardware of the Pulse as it Width Trigger Module. (If you want to learn the detate please refer to the Specification of the Pulse Width Trigger Module.) Set the trigger condition as "Don't Care" See Section 4.1 for detailed instructions. Set the trigger condition as "High" See Section 4.1 for detailed instructions.					
Tip: It is not necessary to register can be used for free. Don't Care High Low	on) single channel, and the signal in this channel can the triggered in the predetermined range. However, the function is required to use with the hardware of the Pulse as it Width Trigger Module. (If you want to learn the detate please refer to the Specification of the Pulse Width Trigge Module.) Set the trigger condition as "Don't Care" See Section 4.1 for detailed instructions. Set the trigger condition as "High" See Section 4.1 for detailed instructions. Set the trigger condition as "Low" See Section 4.1 for detailed instructions.					
Tip: It is not necessary to register can be used for free. Don't Care High	on) single channel, and the signal in this channel can be triggered in the predetermined range. However, the function is required to use with the hardware of the Pulse as it Width Trigger Module. (If you want to learn the detar please refer to the Specification of the Pulse Width Trigg Module.) Set the trigger condition as "Don't Care" See Section 4.1 for detailed instructions. Set the trigger condition as "High" See Section 4.1 for detailed instructions. Set the trigger condition as "Low" See Section 4.1 for detailed instructions. Set the trigger condition as "Low" Set the trigger condition as "Rising Edge"					
Tip: It is not necessary to register can be used for free. Don't Care High Low Kising Edge	on) single channel, and the signal in this channel can be triggered in the predetermined range. However, the function is required to use with the hardware of the Pulse as it Width Trigger Module. (If you want to learn the detate please refer to the Specification of the Pulse Width Trigger Module.) Set the trigger condition as "Don't Care" See Section 4.1 for detailed instructions. Set the trigger condition as "High" See Section 4.1 for detailed instructions. Set the trigger condition as "Low" See Section 4.1 for detailed instructions. Set the trigger condition as "Low" See Section 4.1 for detailed instructions. Set the trigger condition as "Rising Edge" See Section 4.1 for detailed instructions.					
Tip: It is not necessary to register can be used for free. Don't Care High Low	on) single channel, and the signal in this channel can be triggered in the predetermined range. However, the function is required to use with the hardware of the Pulse as it Width Trigger Module. (If you want to learn the detar please refer to the Specification of the Pulse Width Trigg Module.) Set the trigger condition as "Don't Care" See Section 4.1 for detailed instructions. Set the trigger condition as "High" See Section 4.1 for detailed instructions. Set the trigger condition as "Low" See Section 4.1 for detailed instructions. Set the trigger condition as "Low" Set the trigger condition as "Rising Edge"					



Either EdgeSet the trigger condition as "Either Edge"See Section 4.1 for detailed instructions.

Reset

📲 Trigger Property ...

Reset the trigger condition.

Pot A	
Pot B (Mirc1, Max 65535)	
The second secon	
Port C	
TTL 1.5 M	
Port D	
TTL 1.5 M	

Fig 3-33: Set Trigger Content

See Section 4.1 for detailed instructions.

Trigger Level

The voltage level that a trigger source signal must reach before the trigger circuit initiates a sweep.

There are 4 ports available; each port has the ability to assign different voltages to meet the users' requirements.

Use the pull-down menu to choose between TTL (default TTL), CMOS (5V), CMOS (3.3V), ECL and User Defined (choose the value of the Trigger Level – 6.0V to 6.0 V).

50% 💌	🐐 🐳 Page	1 🔻	Count	1	-
(1)		(2)		(3)	

Fig 3-34: Trigger Position, Trigger Page, Trigger Count

(1) Represents the Trigger Position of a memory page.

(2) Represents the Trigger Page.

(3) Represents the Trigger Count.

Trigger Pagel	C Delay Time and Clock
Trigger Page	Trigger Delay Time
1 (Mirc1, Max 8192)	(Mirc10us , Marc167.76191s)
Trigger Position	Trigger Delay Clock
50%	[1 (Mirc1.Max:16776191)
T Pos = Ons , Start Pos = -10.23m	ns , End Pos = 10.25ms
Note: When more than one trigge	r pages are selected, the trigger bar disappears fr

Fig 3-35: Set Trigger Delay

See Section 4.1 for detailed instructions.

Tip:

Tip:

lcon

*

÷.

N/A

N/A

Tr	igger Delay
lcon	Description
N/A	Trigger Delay

Trigger Content Setup

Decrease

position

Description

trigger position

Increase trigger

Trigger Page

Trigger Count



Trigger Delay 10us

Fig 3-36: Set up Trigger Delay clock under time display.

Trigger Delay	1000
---------------	------

Fig 3-37: Set up **Trigger Delay** clock under sampling site display.

The **Trigger Delay** setting in **Tool Box** equals to that in the above dialog box.

Tip:			Trigger Property	×
	Tri	igger Range	Trigger Content Trigger Delay Trigger Range	
-	lcon	Description	P Activate Trigger Range	
-	N/A	Trigger Range	Time Sample	
			OK Cancel Default Help	
			Fig 3-38: Set Trigger Range	

4. Run/Stop





Fig 3-40: Run/Stop Tool Box

Menu Bar: Run/Stop

	Menu Item		Detail Menu & Dialog Box
	Single Run	F5	Click to run once. See Section 4.1 for detailed instructions.
_	Repetitive Run	F6	Click to run continuously until the Stop button is clicked. See Section 4.1 for detailed instructions.
_	Stop	F7	Click to stop the repetitive run. See Section 4.1 for detailed instructions.



5. Data

Select an Analytic Range		
🧰 Noise Filter		
🔯 Bus Width Filter		
Data Contrast		
👪 Find Data Value	Ctrl+F	
💻 Find Pulse Width		
↓ To the Previous Edge	F11	
♦] To the Next Edge	F12	
Go To	•	T Go To T Bar T
+2 Add Bar	Alt+A	A Go To A Bar A
<mark>≓</mark> ¥ Delete Bar…	Alt+B	B¥ Go To B Bar B
X Zoom	E	Go To More
🖑 Hand	Н	
📐 Normal	ESCAPE	Binary
N Zoom In	F9	Decimal
	F9 F8	Decimal (Signed)
K Zoom Out		✓ <u>H</u> exadecimal
💥 Show all Data	F10	ASCII
⊢ Previous Zoom	Ctrl+Z	Gray Code
Data Format	•	Complement
Waveform Mode	Þ	Square Waveform
List Data Mode	•	Sawtooth Waveform
		✓ All Data
		Sampling Changed Dot(Compression)
		Data Changed Dot(Compression)
		east changed bet(compression)

Fig 3-41: Data Menu

🔌 💱 🖑 🎞 🖼 🛛 100%	-		A ¥ Ba⊨	B≱ Ba⊨	T ≹ Ba⊨	+ 2 8a⊨	闁	l 	\$∫
Fig 3-4	42: Data T	ool Box							



Menu Bar: Data

Menu Item	Detail Menu & Dialog Box
🔀 Select an Analytic Range	Check the box to enable the Analytic Range to be changed by dragging the Ds and Dp bars with the left mouse button.
	Noise Filter: It can filter 0~10 Clock's positive pulse
	width or negative pulse width signal.
	Noise Filter
ning Noise Filter	Noise Filter:
	OK Cancel

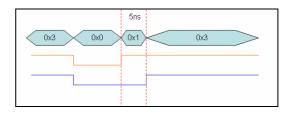
See Section 4.8 for detailed instructions.

	Bus Width Filter	×
	Bus Width Filter	-
🔯 Bus Width Filter	OK Cancel	

Fig3-44: Bus Width Filter

Select the check box to activate the function of the Bus Width Filter in the dialog box, and then users can input the corresponding value of the width to be filtered in the right edit box. Input the time value of the width when the display is in the Time Display or the Frequency Display, and the unit is based on time, such as s, ms, us, etc.; if the inputted value is out of the range, it will switch to the best time value in range. Input the clock value of the width when the display is in the Sampling Site Display, and the range of the input is from 1 to 65535.

For example, after activating this function, and then input the value, 5ns. The Bus Data which is less than or equal to 5ns will be filtered as the figure below:





Contrast...

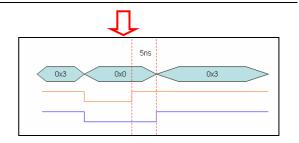


Fig3-45: Before and After Filtering

Basic Film	LaDoci	Digities files horizontal
Contract File:	Iačori	E philipping and make
Contrast Begin		Contrast and Contr
Contrast Slates Contrast Result		Error Rat.

Fig3-46: Data Contrast

Data Contrast: It is used to contrast the difference for the two files of the same style. One is the Basic File, and the other is the Contrast File. The contrast can display the difference between the Basic File and the Contrast File.

		Waveform-Find
👪 Find Data Value	Ctrl+F	Activate the function of Chain-Data-Find Bus/Signal Name: Bus1 Vext Previous Close
		Bus Item: Find: Min Value: Max Value:
		Start = 0 F
		Start At: End At: When Found: Statistics
		Ds Dp A Statistics
		0
		Fig 3-47: Waveform-Find Dialog Box without Activate
		the Function of Chain-Data-Find
		Use the pull-down menu to select the Bus/ Signal
Tip:		Name:
Remember the final condition	s:	The list of Find depends on whether it is a Bus or
When the find function is used	d, the	Signal that is being searched in:
function of displaying the final		Bus – Choose among =, !=, In Range and Not In

conditions is added. When you have closed the Waveform-Find dialog box, and you want to find the set conditions, you can open the Waveform-Find dialog box again for the system has saved the last set conditions.

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Range (enter the value for Min Value and Max Value).
Signal – Choose among Rising Edge, Falling Edge,
Either Edge, High and Low.
Start At - Choose the position to start our search by selecting one of the following:
Ds, T, A, B, etc. (select from the pull-down menu).
When Found - Choose A, B or other bars to mark the

position where it is coincident with the set conditions. **Statistics** – Show the number of instances of the

search results.

Note: It is available only when searching through a Bus.

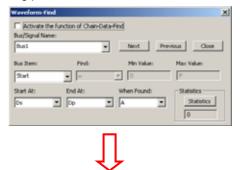
Waveform-Find				×
Activate the fur	nction of Chain-Data	-Find		
Bus/Signal Name:				
Bus1	•	Next Pre	vious Close	
example,0X32,0X45		ma to compart them, fo ds to add the packet na , DATA:0X20.		-
Start At:	End At:	When Found:	Statistics	
Ds 💌	Dp	A 💌	Statistics	
			0	

Fig3-48: Waveform-Find Dialog Box with Activate the

Function of Chain-Data-Find

Tip:

The function of Chain-Data-Find is mainly for finding the data in the packets of Bus and Protocol Analyzer which have some serial data. For example, it can start finding with the serial packet segments (there are 0X01, 0X02 and 0X03) in the Bus. It improves the efficiency of Data Find. See the following process:





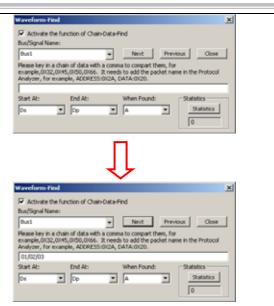


Fig 3-49: Process of Activating the Function of



Fig3-50: Function of Chain-Data-Find Displayed on

the Waveform Window

ignal Name:		Next Previous Close
A0 ind:	Min Pulse Width:	Max Pulse Width: Statistics
In Range 💌	1	65535 Statistics
tart At:	End At:	When Found: 0
Ds 💌	Dp 💌	A V

	Fig3-51: Pulse Width-Find Dialog Box
📮 Find Pulse Width	Signal Name: It can select the single channel for Find.
	Find: It can select the Find conditions which are "In
	Range", "Min Value", ">", "<" and "=". When users
	select the option of "In Range", they can input the value
	of the Min Pulse Width and Max Pulse Width between
	1 and 65535 and find the Pulse Width in range. When
	users select the "Min Value", they can find the Min
Tip:	Pulse Width for the present single channel. When
This function is mainly used for finding	users select the options ">", "<" and "=", they can input

Chain-Data-Find

the pulse width in a single channel and the single channel of a Bus. It improves the efficiency of finding the Pulse Width for engineers and strengthens the Find function of the Logic Analyzer.

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the value of the Pulse Width between 1 and 65535 and find the Pulse Width in range.

Start At: Select the Start point of Find. The selectable items are all Bars; the default is the Ds Bar.

End At: Select the End point of Find. The selectable items are all Bars; the default is the Dp Bar.

When Found: Select a Bar to mark the found Pulse

Width. The selectable items are all Bars; the default is A Bar.

Statistics: It can count the number of Pulse Width in the present range.

Next: It can find the next Pulse Width.

Previous: It can find the previous Pulse Width.

For example: Find in the A1 channel; the Pulse Width is equal to "20us"; take the A Bar as the mark. See the below figure:

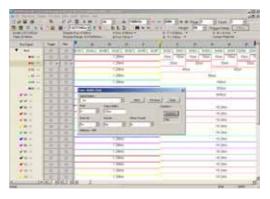


Fig 3-52: Pulse Width-Find on the Waveform Window

14 To the Previous Edge	F11	Go to the previous edge sweep of the indicated signal.
♦∫ To the Next Edge	F12	Go to the next edge sweep of the indicated signal.

	Go To T, A, E	3, or Go To More
	145.022	145.032 230.043 435.065 589.087 725.198
	261450	
	261445	254 48 127 48 47 32 32 48
		393017
		293017
		293017
		283017
	2	283017
		393017
•		383017
		393017

Fig 3-53: Go To T Bar; T Bar will be displayed in the center of the waveform area.

Go To



Tip:

Ţ

<u>A</u>

B

A

в

Select an Analytic Range Noise Filter ... Bus Width Filter... Data Contrast... Go To T Bar Т (1)Find Data Value ... 幵 Ctrl+F A Go To A Bar Find Pulse Width... ►(2) To the Previous Edge F11 14 Go To B Bar В ►(3) To the Next Edge F12 **⇒**[Go To Go To T Bar Go To More... Add Bar. Alt+A Go To A Bar A. Delete Bar.. Alt+B Bat B Go To B Bar (1) Press T, go to T Bar. Ņ. Zoom Е Go To More.. (2) Press A, go to A Bar. Hand н (3) Press B, go to B Bar. R Normal ESCAPE ų Zoom In F9 🖌 Zoom Out F8 Show all Data F10 왮 ŝ Previous Zoom Ctrl+Z Data Format • Waveform Mode • List Data Mode •

Fig 3-54: The selected bar will be shifted to the center of the waveform area.

Add Bar... Alt+A

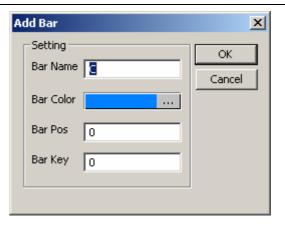
Add user defined bars.

- 1. Click the above menu item from Data menu, or click Add Bar icon from Tool Bar.
- 2. Give a Bar Name, define a Bar Color, and set a Bar Position.
- 3. Define the Bar Key with the number between 0 and 9.

Tip:

The number shortcut is set in the Add Bar dialog box. Every new bar can be filled in one number which is used to find the required bar faster; the default number of the new bar is 0. It is noticed that once the number key is set, it can't be modified, and each new bar can named with the same number, that is to say, one number can name many bars.

For example, users can set the number 3 as the shortcut key. When users press the number 3 key, the C Bar will be displayed in the centre position of the screen.





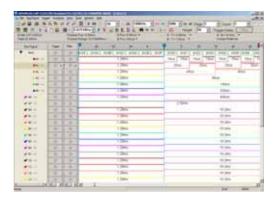


Fig3-56: Add a Bar with the number between 0 and 9.



– 🛃 Delete Bar...

Alt+B

Delete a user defined bar.

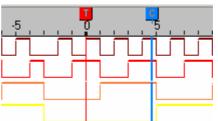
- 1. Click the above menu item from **Data** menu, or click **Delete Bar** icon from **Tool Bar**.
- 2. Select a user defined bar, and click

on Delete.

3. Delete the selected Bar with the **Delete** key on the **Keyboard.** Use the mouse to select the added bar and press the **Delete** key on the keyboard to delete the bar.

C	Delete
	Close

Fig3-57: Delete Bar Dialog Box



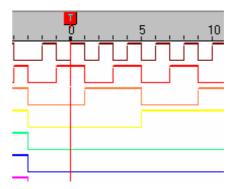


Fig 3-58: Delete a selected Bar.

🕅 Zoom E

Tip:

A Zoom-In or a Zoom-Out view will be centered in the Waveform Display Area, and the new zoomed view will be sized according to the available space on the display.

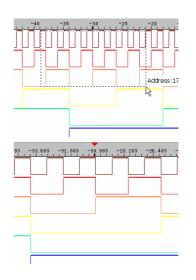


Fig 3-59: To **Zoom In**, left click and drag the mouse/point from left to right.



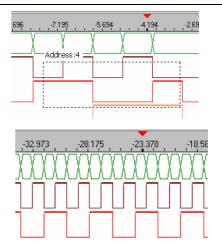


Fig 3-60: To **Zoom Out**, left click and drag the mouse/point from right to left.

a set set and	1224	Sec. 1		L'ALTERNA T	A ALLOW T
A			at Streeting Startings	B.Trobby P	COMPARENTS
Sector 1	100	-	P	1	# . #
			* *** *** *** *** *** ***	mm (+++) mm (-m	
		100	1384	the THE TWO IS AND	
10.00	1.00.4	1.00.00	1.28ms	See See	Ten
1440.11		-	12844	- 404	Aba
(146-14)		100	1 pinne		9400
1000	1.00	1.00	1.5866		1000
		10.0	1 1944	Tree Dire	100m
640		10.4	1.1844	0.111.0	- 1000
863		- 16. 3		1.0mm	
e = 1	10.1	1.0	1.3840	A CONTRACT OF	18.3mg
10.0		100	1.19-0		10.240
		100	13944		14.3%
		1.001	1.2000		18.000
6 m -	1.00	100.0	11000		10.000
22		1.1	1 (Bee).		18:344
1		10	1.2844		18:240
100		-	1344		10.040
144	1.00	1.0	139m)	1	10.04
FR.1		100	1.38%		10,000
		1923	1,2800		14 link

When users activate the **Zoom** to zoom in / zoom out the selected area, the Tooltip on the right corner of the bottom will display the Time, Clock or Address of the selected area. When selecting the Zoom function, and users are pressing and dragging the left key, the information on the right corner of the bottom will be changed and updated with the width of the selected area. And the information is displayed on the right corner of the bottom in the way of Tooltip. When users loosen the mouse, the information will disappear.

Tooltip:

Time/Frequency Sample: xxx (time)

/ns (unit)

Address: xxx (There is no unit with the

address.)

		-10 -5 0 10us
🖑 Hand	н	20us
		EM
	Fig 3-62	2: Click Hand , and then press and hold the left key to drag.

Fig 3-61: To display the Tooltip, left click and drag the mouse/point from right to left or from left to right.



 Normal
 ESCAPE
 Reset the mouse function to the system default.

 Image: State of the system default.
 Image: State of the system default.

 Image: State of the system default.
 Image: State of the system default.

 Image: State of the system default.
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 Image: State of the system default.
 Image: State of the sys

Tip:

Zoom In and Out can be switched by changing the percentage value in the pull-down list.

1. The system can set the value of Zoom In and Out:

The default unit is µs. When zooming in, it will be automatically changed to ns. When zooming out, it will be changed to ms, s or ks.

2. Pull-down Menu:

There are thirty scales. The maximum zoom in and out is the cycle of each grid, 0.0001piece. The minimum zoom in and out is the cycle of each grid, 1,000,000,000.

Zoom in and out (the proportion): with each grid being the cycle, the zoom in and out (%) is 100%. The time of Zoom In and Out counts by the clock of each grid (sample frequency). For example:

(1) Each grid is being a cycle; the zoom in and out is 100%. The time of Zoom In and Out will be presented by the clock of each grid X (1/sample frequency).

(2) Each grid stands for the clock of 100 pieces, the zoom in and out is 1% and the time of Zoom In and Out will be displayed by the cycle of each grid X (1/sample frequency).

Display Pos:0 Display Range:-250 ~ 25 -200 - 150 -150 -200 - 150 Fig 3-63: Normal Status □ splay Pos:0

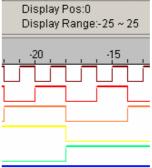


Fig 3-64: Result from Normal to Zoom In

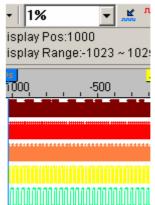


Fig 3-65: Result from Normal to Zoom Out



Show all Data	F10	Fig 3-66: Show all Data
🖌 Previous Zoom	Ctrl+Z	Return to the last zoom.
Data Format	•	Binary Decimal Decimal(Signed) ✓ Hexadecimal ASCII Gray Code Complement

Fig3-67: Data Format

Show numerical information in Binary, Decimal,

Decimal(signed), Hexadecimal, ASCII, Gray Code, or

Complement.



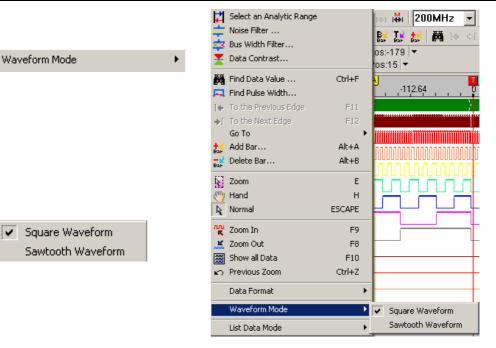


Fig 3-68: Square Waveform

H	Select an Analytic Range		
ЩШ.	Noise Filter		B <u>2 T¥ +2</u> ∰ [♦ ♦]
*	Bus Width Filter		
÷.	Data Contrast		os:-179 ▼ los:15 ▼
B B	Find Data Value	Ctrl+F	T
	Find Pulse Width		-28.16
14	To the Previous Edge	F11	
	To the Next Edge	F12	
	Go To	•	ΛΛΛΛΛΛΛΛΛΛ
+2 Bat	Add Bar	Alt+A	
	Delete Bar	Alt+B	
Bar	Doloco Bal III	HICTO	
1	Zoom	Е	
en	Hand	н	
R	Normal	ESCAPE	
-			-
лл К	Zoom In	F9	
L.	Zoom Out	F8	L 4
**	Show all Data	F10	
5	Previous Zoom	Ctrl+Z	
			-
	Data Format	•	
	Waveform Mode	Þ	Square Waveform
	List Data Mode	•	Sawtooth Waveform

Fig 3-69: Sawtooth Waveform



List Data Mode

Tip:

The data for list mode are so many, to be convenient for users, that there is adding a List Data Mode function. The formats for the List Data Mode are All Data, Sampling Changed Dot (Compression) and Data Changed Dot (Compression).

۲

All Data: It is the present display mode.

Sampling Changed Dot

(Compression): Take the sampling changed dot as the compression data reference dot.

Data Changed Dot (Compression):

Take the present data change dot as the compression data reference dot.

H	Select an Analytic Range		ÞI	∲ I∰	ı 2	00M	Hz	•	n nn	nnr	50
ŵ	Noise Filter		B	🖌 Tı	è <mark>∔</mark> ≧ Bat	-	14		8	•	BU
*	Bus Width Filter			s:-178			-			A-	T
X	Data Contrast			s:15						В-	
酶	Find Data Value	Ctrl+F		B1	B2	вз	В4	B5	B6	В7	0
딦	Find Pulse Width		ř		102	0.0				1	
l+	To the Previous Edge	F11	н		1		1	.	.	-	Г
•[To the Next Edge	F12									
	Go To	•	ŀ	0	0	0	0	0	0	0	
+ ≧ Bar	Add Bar	Alt+A		0	0	0	0	0	0	0	
Bar	Delete Bar	Alt+B	Þ	0	0	0	0	0	0	0	
	Zoom	E		0	0	0	0	0	0	0	
3	Hand	н	H	n	n	n	n	n	n	n	
R	Normal	ESCAPE	F	0	0	0	n n	n n	0	0	
ллі K	Zoom In	F9		0	0	0		n n	0	0	
, Ke	Zoom Out	F8	E								
	Show all Data	F10	ŀ	0	0	0	0	0	0	0	
K)	Previous Zoom	Ctrl+Z	ŀ	0	0	0	0	0	0	0	
	Data Format	•	ŀ	0	0	0	0	0	0	0	
	Waveform Mode	•	P	0	0	0	0	0	0	0	
	List Data Mode	•		All 0	Data		1				
	1 1 0 0 0			San	npling	Chan	ged D	ot(Co	mpres	sion)	
					a Cha					. '	

Fig 3-70: List Data Mode: All Data, Sampling Changed Dot (Compression) and Data Changed Dot (Compression).



6. Tools

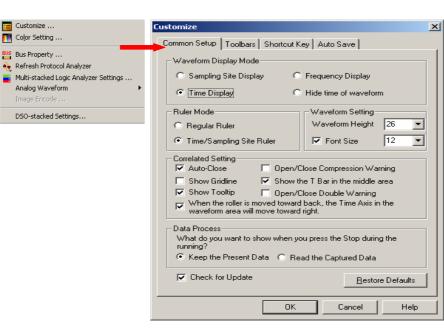


Fig 3-71: Tools Menu



Fig 3-72: Tool Tool Box



Menu Bar: Tools

Menu Item	Detail Menu & Dialog Box
	Customize X
	Common Setup Toolbars Shortcut Key Auto Save
Customize	Waveform Display Mode
Customize	O Sampling Site Display O Frequency Display
	C Time Display C Hide time of waveform
	Ruler Mode Waveform Setting
	C Regular Ruler Waveform Height 22 💌
	Time/Sampling Site Ruler Font Size
	Correlated Setting Image: Correlated Se
	When the roller is moved toward back, the Time Axis in the waveform area will move toward right.
	Data Process What do you want to show when you press the Stop during the running? C Keep the Present Data C Read the Captured Data
	Check for Update <u>R</u> estore Defaults
	OK Cancel Help
	Fig 3-73: Customize Dialog box
	See Section 3.4 for detailed instructions.
	Customize X
	Common Setup Toolbars Shortcut Key Auto Save
	Toulars ✓Standard
	▼ Trigger
	I I I I I I I I I I I I I I I I I I I
	✓ Trigger Content Set
	☑ Display Mode ☑ Windows
	Mouse Pattern
	I Zoom I Data
	☑ Height
	✓ Trigger Delay □ Font Size
	✓Data Contrast/Screen Display
	OK Cancel Help
	Fig 3-74: Toolbars Setting



Customize		×
Common Setup Toolbars Sh	nortcut Key Auto Save	
Commands:	Current Keys:	
Add Bar. Capture Window Close	Alt+A	Assign
Delete Bar Down End		Remove
Esc Export Waveform F2 F3 F3		Reset All
Currently affected to :	Select New Shortcut Key:	
Description:		
+ 🖌 Add Bar Ba⊨		
	OK Cancel	Help

Fig 3-75: Shortcut Key Setting

Customize X
Common Setup Toolbars Shortcut Key Auto Save
I⊄ Activate File Name: LA
Save Path Name: D:\Documents and Settings\123\My Documents\LA
Repetitive Run Time Interval: Data Display Menu Renewal Mode C Open the first file after stopping the Run
Default
OK Cancel Help

Fig 3-76: Auto Save Setting

See Section 3.5 for detailed instructions.



[Color Setting ...

xI

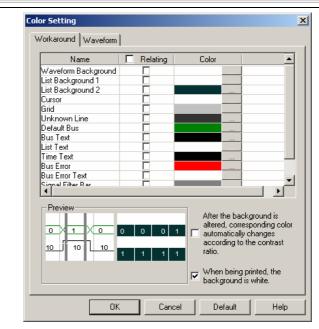


Fig 3-77: Color Setting

See Section 3.6 for detailed instructions.

	our reperty	
	Bus Setting	
	C Bus	Color Config
	Activate the Latch Function	A0 👻
		Rising Edge
	- Protocol Analyzer Setting	
	Protocol Analyzer	Parameters Config
	C ZEROPLUS LA 3-WIRE MODULE VI.0 C ZEROPLUS LA AC97 MODULE VI.0 C ZEROPLUS LA AC97 MODULE VI.0 C ZEROPLUS LA ANTI-METICAL LOGI C ZEROPLUS LA CAN 2.08 MODULE VI C ZEROPLUS LA CORPACT Flash 4.1 M C ZEROPLUS LA CORPACT Flash 4.1 M C ZEROPLUS LA CORPACT Flash 4.1 M C ZEROPLUS LA CONSTIMASE MODULE C ZEROPLUS LA CONSTIMASE MODULE VI.	:00(CN01) IC MCDULE V1.51.00(CN01) 00(CN01) 1.32.00(CN01) .31.00(CN01) OULE V1.01.00(CN01) E V1.00.00(CN01)
	l	OK Cancel Help
	Fig 3-78: I	Bus Property
	Bus: Activate the function of	analyzing the Bus.
5 for detailed	Color Configuration: Open box to set the conditions for t	•
ons.	Activate the Latch Function	n: Activate the latch function

Protocol Analyzer: Activate the function of analyzing the Protocol Analyzer.

Use the DsDp: Use the Ds and Dp to help analyze the Protocol Analyzer.

Find: Find the desired Protocol Analyzer module. Users can input the Protocol Analyzer name to quickly find the Protocol Analyzer module from many Protocol Analyzers. After inputting the first character of the name in the Find box of Bus Property dialog box, the corresponding module will be displayed in the Protocol Analyzer list box according to the input character. See the figure below:



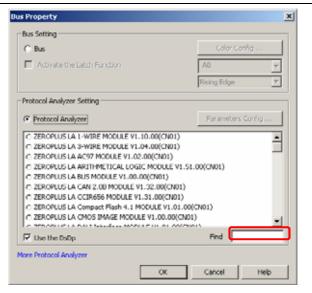


Fig 3-79: Find Editor Box

When you input "I" in the Find editor box, the Protocol Analyzer list displays all Protocol Analyzers with the initial character of "I"; see the below picture:

CBus	Color Config
Activate the Latch Function	A0
	Rising Edge
Protocol Analyzer Setting	
Protocol Analyzer	Parameters Config
C ZEROPLUS LA 120(EEPROM 24LCS61/24U C ZEROPLUS LA 120(EEPROM 24L) MODULE C ZEROPLUS LA 120 MODULE V2.02.00(CN0 C ZEROPLUS LA 125 MODULE V1.13.00(CN0 C ZEROPLUS LA 1507816 LIART MODULE V1	V1.31.00(CN01) 1) 1)
C ZEROPLUS LA 12C(EEPROM 24L) MODULE C ZEROPLUS LA 12C MODULE V2.02.00(CN0 C ZEROPLUS LA 12S MODULE V1.13.00(CN0)	V1.31.00(CN01) 1) 1)
C ZEROPLUS LA 12C(EEPROM 24L) MODULE C ZEROPLUS LA 12C MODULE V2.02.00(CN0 C ZEROPLUS LA 125 MODULE V1.13.00(CN0)	V1.31.00(CN01) 1) 1)
C ZEROPLUS LA 12C(EEPROM 24L) MODULE C ZEROPLUS LA 12C MODULE V2.02.00(CN0 C ZEROPLUS LA 12S MODULE V1.13.00(CN0 C ZEROPLUS LA 1507816 LIART MODULE V1	V1.31.00(CN01) 1) 1) 02.00(CN01)

🍓 Refresh Protocol Analyzer	Refresh Protocol Analyzer data.
1	See Section 4.10 for detailed instructions.

	Multi-stacked Logic Analyzer Settings	×
	Ctivate Stack	
	Stack Type	
	Memory Stack	
	Channel Stack	
	Please select the Logic Analyzer for stacking	
	M1 S/N:000000-0000	
	□M2 S/N:000000-0000	
	M3 S/N:000000-0000	
i-stacked Logic Analyzer Settings	□M4 S/N:000000-0000	
	Synchronous Channel	
	Synchronous Trigger Condition	
	Rising Edge	
	OK Cancel H	elp

Fig 3-81: Multi-stacked Logic Analyzer Settings Dialog Box See Section 4.12 for detailed instructions.

Analog Waveform	
🚧 Single Analog Display 🚽	

Mixed Analog Display

Analog Waveform

The function of Analog Waveform means that the Display Mode of Bus Data is not the Pure Data Mode, while it displays data change with the curve which looks like a waveform, which, in fact, is a curve to describe the data change. So it is called the Analog Waveform.

The Analog Waveform can be divided into two kinds, namely, Single Analog Display and Mixed Analog Display, see the figures as below:

MACHINE STREET	- Concerned	ALL STREET	L D L M	2 + EL 2 - 1-100 2 - 1-100	nage (PA	A-BA MIL	4
darland "	Tasi 2 Per 1	A		(COL)	and the second		
1. (m)	10.5	101010000000	11111111111111		I I I I I I I I I I I I I I I I I I I	10101000	1111111
	100.8.00-						
	「田口里」目白						
	THE PARTY			1.00			
· · · · · · · · · · · · · · · · · · ·	CHOICE WAS	HELP IL	1824		Hike		- NEILA
#H	100.00	1984		3264		_	104
		biller			8454		
88-		- 120mi			12784		
	· · · · · · · · · · · · · · · · · · ·			18	2714		
	10.10						
	10000			18	204 204		
	10.2.10						
	A 2 A				200		
48.0					2mi		
4.00	10.2.2.2				(mag)		
1800	1.00			19	201		
****				14			
((())) () () () () () () ()	10.1.1				384		
# 12 10					2mi		
1000	COMPANY OF COMPANY				244		

Fig 3-82: Single Analog Display

Tip:

M

When the function of Analog Waveform is activated, the Analog Waveform will be displayed in the waveform area of the Bus's sub-channel and take the space of four channels. And four sub- channels won't draw the waveform. It notes that the sub-channel of the Bus must be more than four channels.



B (2) & 5	1			5.2+2/MO.	Ci Inager	14 1 1	A Dane -	1
100.25 4946		1		faritie#1	8 Tarthe +			
darfield .	(hasi-	2.000	And American State	A		First	Can Bear	180
Y	100.5	1.00	110.000 UIIII	TELEVISION OF	DOULL	0101010		LTTT:
	1.00	2 H .	PARARA	annannar	hhhh	AND	20000	100
100 m			and the strend the	All and the all and the	20,000,000	and the fit	podition di	20.00
	1.00	1.11	ALL ALL ALL	the area and	474 445	anto atta	abs and	-dist
1.00	100.1	1.11	MA BA	Sta Mbr	Bhe	She	- Black	
	1.000		Miles .	talka.		ile .		and a
# M	100		1,044		25a4			1244
100-			141.0			and a		
100	1		1204			12794		
440			-		10.276			
	1.10				10.204			
	1 10				19.2%			
	1.00	1.00			10.004			
400	10.1	1.1			14.2%			
	-				19,200			
da -		1 2			10.204			
. 600		1.0			19.2m			
	-	-			10.2%			
					14 percent			
	1.000	1.10						

Fig 3-83: Mixed Analog Display

Image Encode ...

Decode the data of Protocol Analyzer and show it in image (the Protocol Analyzer shall support this function).

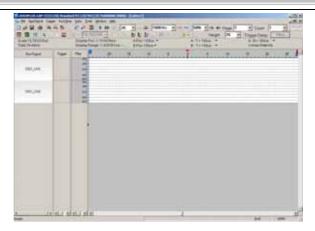
Thannel V/Div Setting			
DSO_CH1 V/Div: SV/D	v DSO_C	DH2 V/Div: 2V/Div	-
DSO_CH3 V/Div: 2V/De	v 💌 DSO_C	DH4 V/Div: 2V/Div	*
hannel Setting			
Conly display DSO			
🔽 DSO_CH1 🔽 DSK	o_onz ₹ Dso_o	она 🗵 разо_сн	н.
	***	•••	-
Channel Height Setting			
DSO_CH1 Height: 80	D50_CH	12 Height: 80	
DSO_CH3 Height: 80	DSO_CH	H Height: 80	
Master			
Logic Analyzer	C pso		

DSO-stacked Settings...

Channel V/Div Setting: Users can select the Options, 3V/Div,2V/Div, 1V/Div, 500mV/Div, 200mV/Div, 100mV/Div, 50mV/Div,20mV/Div, 5mV/Div and 2mV/Div.

Channel Setting: Users can set the DS0_CH1, DS0_CH2, DS0_CH3, DS0_CH4, the captured waveform will be displayed on the LA Software; meanwhile, the color of CH can be changed. When selecting the item, Only display DSO, only the activated DSO CH can be displayed on the waveform. The A0~A7 can't be displayed, see as below figure.





Channel Height Setting: Set it from 30 to 400. DSO Settings: when the button is pressed, the below box will be displayed.

Master: Set the Master to be LA or Oscilloscope according to the hardware usage mode.

scilloscope Brand:	Tektronix	Y	
onnect Mode			
💽 USB	${f C}$ TCP/IP	${f C}$ auto	
🔲 Use the Agilen	: GPIB-to-USB Sw	itching Card	
tack Parameters			
Current Connect Model:	TDS 1002B-SC		
Sampling Frequency:	100000.00	Hz	
Stacking Delay:	0	Ps	
Trigger Position:	50	- %	
Trigger Channel:	External	- 1.00	- v
Trigger Type			- 10.
Activate			
🗭 Trigger Edge	Rising Edge	-	
C Video	All Lines	-	
C Pulse	<	- 100	ns
Polarity: Ne	q 💌 Uppe	er Limit: 2.0	ns
Trig When: Ou	tside 💌 Lowe	er Limit; 2.0	ns

Oscilloscope Brand: User can select the oscilloscope brand to stack, such as Tektronix. Then click the Connect button to show the oscilloscope model, None will be displayed if no oscilloscope is connected.

Connect Mode: Users can select USB, TCP/IP or Auto. If selecting the USB, the oscilloscope will



connect with the PC by USB. If selecting the TCP/IP, the oscilloscope will connect the PC by TCP/IP, and the IP needs to be set the same as the IP of current PC. If selecting the Auto, users can connect without any setting.

Current Connect Model: Display the oscilloscope's name.

Sampling Frequency: It matches with the sec/case spin button of oscilloscope. Its value is the reciprocal of horizontal scale, the range is 1/5ns ~ 1/50s.

Stacking Delay: It is used to align the T Bar and the T Bar of LA when users use the main program to show the oscilloscope's waveform. The range is -1000000ps~+100000ps.

Trigger Position: It matches the horizontal spin button of oscilloscope, the range is 0~100%.

Trigger Channel: It matches the trigger level spin button of oscilloscope, the lever range is -16V~ 16V. **Trigger Type:** The other options is available only after the active option is selected.

A. Trigger Edge: Users can select Rising Edge or Falling Edge.

B. Pulse: Users can select <, >, =, !=; the range is 33ns~10s.

C. Video: Users can select Line, All Lines, Odd Field, Even Field and All Field.

Connect: Click the Connect to link with the oscilloscope, and the Online button will change into Disconnect button.

Users can set the oscilloscope by selecting the options and inputting values, then pressing OK. Note: the Stacking Delay is set into the main program. If no oscilloscope is connected or the oscilloscope disconnects, the whole options under the Stack Parameters are unable. For the above details, please refer to the 4.13.



7. Window

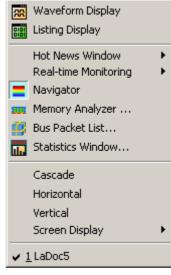


Fig 3-84: Window Menu



Fig 3-85: Window Tool Box

Menu Item	[Detail N	lenu & C	Dialog Box	
	🛵 Elle Bys/Signal Trigg	er Run/Stop	Data Tools	Window Help	
	🗋 🧀 🖬 🍜 🛋	2 🐐 🖓	🕂 📲 ष	🙀 Waveform Display	200
	🕅 📰 📪 💊 😡	0 🖬 🛙	- 5ns	E Listing Display	15 22
	Scale:200MHz Total:10.24us		Display Pos: Display Ran	Real-time Monitoring +	75ns = 75ns =
The Maria Fauna Disalary	But/Signal	Trigger	Filter	Navigator Memory Analyzer	50ng .
👷 Waveform Display	- AQ AQ			Bus Packet List	
	A1 A1			Statistics Window	Fir
	🧳 AZ AZ			Cascade	
	CA 🗗 🏷			Horizontal	
	✓ A4 A4			Vertical	
	🖌 AS AS			Screen Display	
	🥑 A6 A6			✔ 1LaDoc5	
	₫ A7 A7				
	# 80 80				
	# B1 B1				



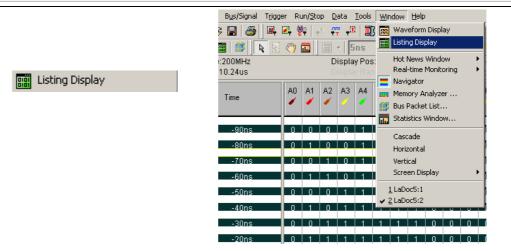


Fig 3-87: Display Signals in Listing.

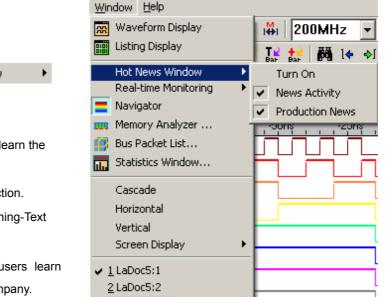


Fig 3-88: Hot News Window and the Pull-down Menu

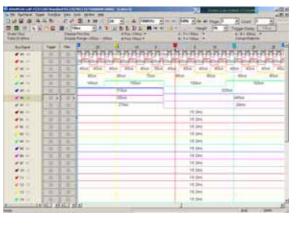


Fig 3-89: Display Hot News Window on the Software

Interface.

Protocol Analyzer MVB_V1.01.00 Publish

Fig 3-90: Running-Text Ads Interface

Hot News Window

Tip:

To let online users learn the latest news, we add the Running–Text Ads Function. **Turn On:** Start the Running-Text

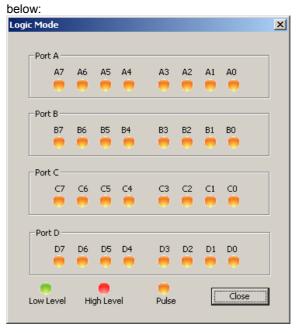
Ads function.

News Activity: Let users learn the activities of our company.

Production News: Let users learn the latest products of our company.

Note:

If both News Activity and Production News are turned on. The Running-Text Ads will play News Activity prior to Production News, and play the news in order; the whole process plays repetitively. Real-time Monitoring: The Level and the Frequency of all the channels can be monitored according to the Real-time Monitoring function of software, which is convenient for users to know the current data status of each channel. There are two display mode, see as



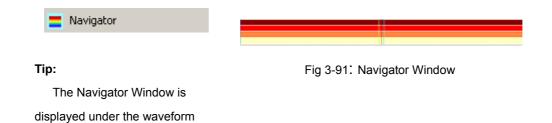
Real-time Monitoring

display area when activating the

Logic Mode Display

requency Mode			2
Port A	Port 8	Port C	Port D
A0 8.8330Hz	80 31.218MHz	C0 29.689MHz	00 6.259MHz
A1 20.44012	81 2.569012	C1 23.041012	D1 22.49901z
A2 20.17199tz	82 12.1629912	C2 24.30901g	D2 27.13904z
A3 5.0660Hz	83 2.844942	C3 10.8790Hz	D3 11.8490Hz
A4 30.55801z	B4 29.90604z	C4 23.507MHz	D4 21.041092
A5 31.62294tz	85 26.2299942	C5 2.598XHz	D5 3.451MHz
A6 24.84801t	86 3.785012	C6 20.1360%	D6 25.72204z
A7 13.4929912	87 10.72704z	C7 9.03989tz	07 32.60001/2
			Close

Frequency Mode Display



Logic Analyzer. The Navigator displays the waveform length of all the captured data; it only can display the waveform of the data of four channels. In the Navigator Window, users can click the Left Key of the mouse to select the waveform randomly. The selected waveform keeps pace with the waveform in the waveform display area. The size of the selection frame is in inverse proportion to the Zoom Rate; the larger the Zoom Rate is, the smaller the size of the selection frame is. Users can also click the Right Key of the mouse to select the displayed channel.

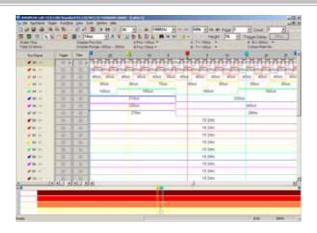


Fig 3-92: Navigator Window under the waveform

display area

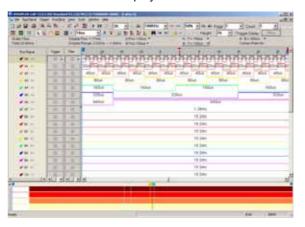


Fig3-93: Blue Frame in the Navigator Window There is a blue frame in the above Navigator Window. Users can click the Left Key of the mouse to select the waveform randomly.

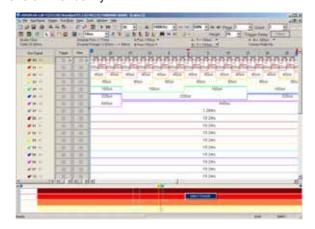


Fig3-94: Select Channel button After clicking the Right Key of the mouse, the Select Channel dialog box will pop up as below.



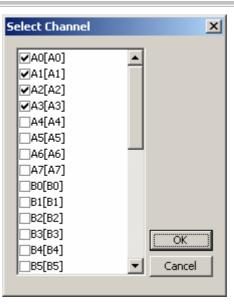


Fig3-95: Select Channel dialog box

In the Select Channel dialog box, users can select the channel which users want to display; users can select four channels at most; the defaulted channels are A0, A1, A2 and A3 (there are four channels in total).



Fig 3-96: **Memory Analyzer** Interface See Section 4.11 for detailed instructions.

🚦 Bus Packet List...

Tip:

Setting: Set up the packet list. Refresh: Click it, the content in the packet list will be refreshed.

Export: Users can use the

fragment to work, record and

analyze the packet list data. As

Export, according to the packet list arrangement, it exports the text file and csv file.

Synch Parameter: Open the Synch Parameter Setting dialog box.

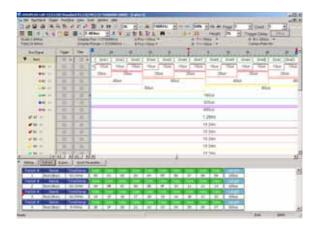


Fig3-97: Display Packet List



Statistics Window	Observation Control Selection Control Selecion Control Selecion C
	Fig3-98: Statistics Window
	See Section 3.3 for detailed instructions.
Cascade	
	Fig 3-99: Cascade Workspace(s)
Horizontal	
	Fig 3-100: Align Workspace(s) Horizontally
Vertical	
	Fig 3-101: Align Workspace(s) Vertically

Fig 3-101: Align Workspace(s) Vertically



Screen Display:

	Screen Display	►
	Double Screen Display	
	First Screen Display	
	Second Screen Display	
_		

When there are two displayers connecting, users can select
🛃, Double Screen Display, to display waveforms on both
two displayers; it is convenient for displaying more
waveforms. 🚺, First Screen Display, or 🔳, Second
Screen Display, can also be selected to display waveforms
on the first displayer or the second displayer.

8. Help

	Logic Analyzer Help	F1
	Keyboard Map	
	Problem Feedback	
ଂ	About ZEROPLUS Logic Analyzer	
	About ZEROPLUS More Protocol Analyzer	

Fig 3-102: Help Menu

Menu Bar: Help

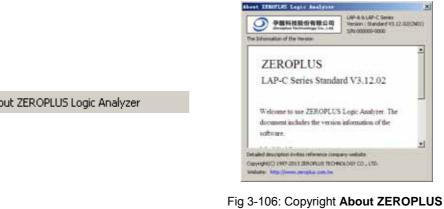
Menu Item		Detail M	enu & I	Dialog Box
		12 mb		
Logic Analyzer Help	F1	Commission Commis	ZEROP	LUS
		 € Trainer of Simple Light the Exception Exception Exception Exception Exception Exception Exception Exception Exception 	使用手册	Locic C
				Trainers Best dialog
		Fig 3-103: Op	en Log i file.	c Analyzer H
		💕 Ber Kay Yaw		
		and the second se		Ali
		Orders	Hotkey	
		Place the A Bar postery Place the B Bar postery Place the T Bar postery Charge to Declare node Charge to Declare node		More execution to others balance More execution to others balance fractions T-Dar to the sectors of a Change the results inside to this Change the results inside to this
Keyboard Map		Place the A Bar postery Place the B Bar postery Place the B Bar postery Place the T Bar poster) Charge to Place Despris Place Part B Bar Bar - Graph	8 2 8 11 00(+3) 00(+3) 00(+3)	More executions to where balance of More executions to where balance of Feasibles 11-back in the careful of a Change the emission marks to the PLA. Also as the careful of deply Careful the animal instance of deply Careful the archite careful of a careful of
Keyboard Map		Place the A Dar position Place the D day position Place the T Dar position Disaget to Enclose nucle Oneget to Hand wate Put A Dar Put A Dar	A T T T T T T T T T T T T T T T T T T T	More executive to where balance More executive to where balance Position 7.25c in the particle of a Change the musule inside to Elec Change the musule inside of depti- Pos Shife with a solid of depti- Pos Shife with a solid of depti- Pos Shife with a solid of depti-

Fig 3-104: The Table of Keyboard Map





Fig 3-105 Feedback Interface



Logic Analyzer

About ZEROPLUS Logic Analyzer

Open the website of Zeroplus Technology

About ZEROPLUS More Protocol Analyzer

to know more modules.

Tip:

The function of Software Version Information Display for ZEROPLUS LA means that the software will open a small window which displays the software version, new functions and bug modifications when activating the software. It is convenient for users to know the information of the present software version.

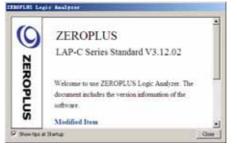


Fig3-107: Software Version Information **Display Window**



Right Key

м	en	ш	Ite	m

Right Key Menu on the Bus/Signal Column

Tip:

The Right Key menu is added on the basis of the Bus/Signal menu. So the function of Sampling Setup, Channels Setup, Bus Property, Group into Bus, Ungroup from Bus, Format Row and Rename are the same as those in the Bus/Signal menu. And the function of the Analog Waveform is the same as that in the Tools menu.

	Detail Menu & Dialog	д вох
<u>.</u>	Sampling Setup	
2 ,	Channels Setup	
BUS	Bus Property	
	Analog Waveform	•
	Image Encode	
	Reverse	
	Group into Bus	Ctrl+G
	Ungroup from Bus	Ctrl+U
	Add Channel	
	Copy Channel	
	Delete Channel	
	Delete All Channels	
	Restore Default Channels	
	Format Row	•
	Rename	

Fig 3-108: Right Key Menu on the Bus/Signal Column

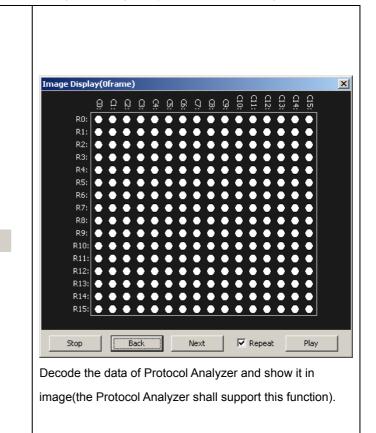
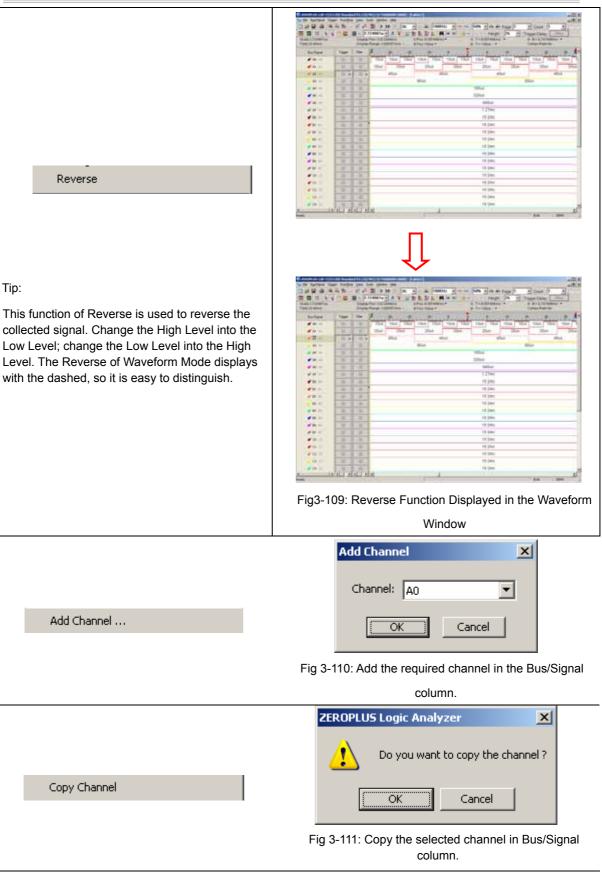


Image Encode ...







	ZEROPLUS Logic Analyzer	×
	Do you want to delete the channel	2
Delete Channel	OK Cancel	
	Fig3-112: Delete the selected channel in Bu	s/Signal
	column.	
	ZEROPLUS Logic Analyzer	×
	All the Buses and channels will be deleted. Do you want to a	:ontinue?
Delete All Channels	Cancel	
	Fig 3-113: Delete all Buses and channels in Bus	s/Signal
	column.	
	ZLROPLUS Logic Analyzer	×
	All the Buses and channels will restore to the default. Do you want to	continue?
	OK Cancel	
Restore Default Channels		
	Fig3-114: Restore the deleted Buses and chan	neis in
	Bus/Signal Column.	
Right Key Menu on the Waveform Area	👸 Find Data Value Ctrl+F	
5	Find Pulse Width	
Tip:	Go To 🕨	
The functions of the right key menu on the	Place	
waveform area are similar to those of the Data	tar Bar →	
	Zoom E	
menu.	- Hand H - R Normal ESCAPE	
The menu adds the functions, such as Place		
Ds and Dp, Add Bar in the waveform display	Show all Data F10	
area.	Previous Zoom Ctrl+Z	

Fig3-115: Right Key Menu on the Waveform Area

Data Format

Color ...

Waveform Mode

Bus Data Color... Bus Single Data Color... ۲

۶



Place	Þ	Place A Bar
🕂 Add Bar		Place B Bar
🔀 Zoom	E	Place Ds Bar
🖑 Hand	н	Place Dp Bar
Normal	ESCAPE	Place More

Tip:

The right key menu on the waveform area adds the function of Place Ds and Place Dp. However the functions are only used after the Ds and Dp bars are activated, otherwise they will be disable. These functions are the same as that of A Bar.

When the mouse is stopped at a special position, click the right key on the mouse, select the Place Ds or Place Dp, the Ds or Dp bar will move to the special position.

For example, Open "Select an Analytic Range", select the special position is "-10", and then select "Place Ds". See the figure in the right column.



Tip:

When the mouse is located at a special position on the waveform area, click the right key to select the Add Bar function; a bar will be added automatically in the special position according to the sequence of the word and color. See the C Bar in the position "5" in the right column.

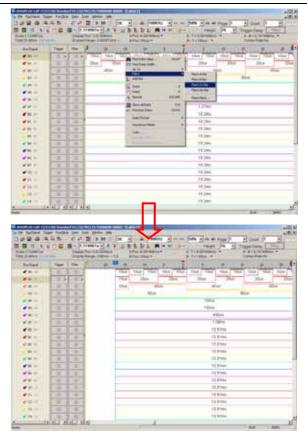


Fig3-116: Place Ds Bar

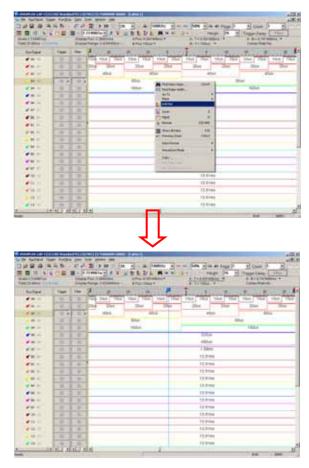


Fig3-117: Add a Bar on the Waveform Area.



3.2 Find Data Value

Find Data Value is a very useful tool to help the user to find data on the received signals.

Step1. Click the find data value 👪 icon; the dialog box of Waveform-Find will appear.

Step2. Using the pull-down menu, select the Bus/Signal Name.

The Bus/Signals listed on the pull-down menu represent the status of the Bus/Signal column as shown in Fig 3-118.



Fig 3-118

Step3. Choose the character for Find. The list of characters depends on whether it is a Bus, Signal, or the protocol analyzer such as I2C, UART, SPI, etc., which is being searched (See Figs 3-119, 3-120, 3-121, 3-122, 3-123, 3-124, 3-125, 3-126 and 3-127).

Bus: Choose among = , != , In Range and Not In Range (Enter the Min Value or Max Value).

Protocol Analyzer: Choose the segments bits of the protocol analyzer (Select the protocol analyzer item and enter the value for Min Value or Max Value).

Signal: Choose among Rising Edge, Falling Edge, Either Edge, High or Low.

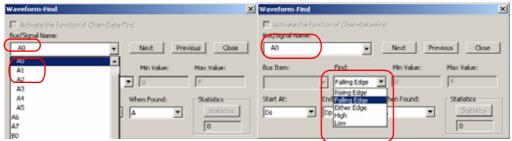


Fig 3-119: Waveform-Find Dialog Box of the Logic Signal

Waveform-Find	×	X Waveform-Find
C Activate the function of Chain-Data-Find		Activate the function of Chain-Data-Find
Bus/Signal Name:		Aug Sagnal Name:
Bus2 • Next	Previous Close	Bus2 Next Previous Close
Dust		
A0 Min Value:	Max Value:	Bus Item: Find: Min Value: Max Value:
A1 00	F	Data 💌 💷 💌 00 F
A3 When Found:	- Statistics	Start At: End
A4 1 0		In Range
A6 Dus2	0	0



Waveform-Find		× Waveform-Fine	1	×
C Activate the function of Chain-Data Dus/Signal Name:	Find Next Previous	Close Bust		iext Previous Close
A0 A1		: Value: Bus Item: Start		Min Value: Max Value:
A2 A3 A4 A5 A6	When Found: St	Start ADDRESS Statistics Read Write	d At: Whe	n Found: Statistics

Fig 3-121: Waveform-Find Dialog Box of the Protocol Analyzer I2C



Waveform-Find		Waveform-Find	đ
Activate the function of Chain-Data-Find		Activate the function of Chain-Data-Find	
Bus/Signa Name:		Pus/Signal History	
	Next Previous Close	A1 Next Previous Close	
6us1 A0	Min Value: Max Value:	Bus Item: Find: Min Value: Max Value:	
	0 F	A-ACK Faling Edge 0 F	
A3 W	en Found: Statistics	Start At: Edge Edge Product Statistics	
A4 A5	Statistics		
A6 A7	0		



Waveform-Find	×	Waveform-Find		×
C Activate the function of Chain-Data-Find		Activate the function of Chai	in-Data-Find	
Bus/Signal Name:		Pus/Signal Name:		
Bus2 Next	Previous Close	Bus2	Next Previous Close	
Busi An Min Value:	Max Value:	Bus Item: Find:	Min Value: Max Value:	
	F	Unknow -	2 0 F	_
A1 A2 When Found:		Linknow 1		-
43	Ratistics	Start d At:	When Found: Statistics	
		Oata D Odd Party	A Statistics	4
A5 A6	0	Step	0	

Fig 3-123: Waveform-Find Dialog Box of the Protocol Analyzer UART

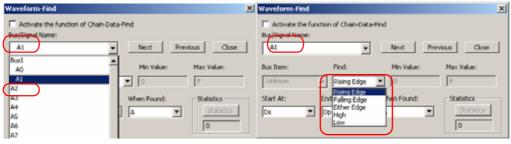


Fig 3-124: Waveform-Find Dialog Box of the UART Signal

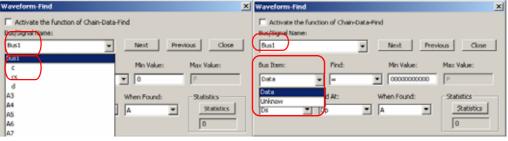


Fig 3-125: Waveform-Find Dialog Box of the Protocol Analyzer SPI

Waveform-Find	X	Waveform-Find
Activate the function of Chain-Data	a-Find	C Activate the function of Chain-Data-Find
Ben/Signal Name:		Bus/Signal Name:
CS .	Next Previous Close	CS Next Previous Close
bust	Min Value: Max Value:	Bus Item: Find: Min Value: Max Value:
d d	00000000000 F	Data r Faling Edge r 0000000000 F
A3	When Found: Statistics	Start At: End Edge hen Found: Statistics
A4 A5	A Statistics	Ds Dp Ether Edge Statistics
A6 A7	0	

Fig 3-126: Waveform-Find Dialog Box of the SPI Signal



Waveform-Find	K Waveform-Find
C Activate the function of Chain-Data-Find	C Activate the function of Chain-Data-Find
Bus/Signal Name:	Bus/Signal Name:
SPI Next Previous Close	SPI • Next Previous Close
Bus Item: Pind: Min Value: Max Value:	Bus Item: Find: Min Value: Max Value:
Data • = • 0000000000 F	Data 👻 In Range 💌 00000000000 F
Data d At: When Found: Statistics	Start At: End in hen Found: Statistics
Ds Dp A Statistics	Ds

Fig 3-127: Waveform-Find Dialog Box of the Bus Item of the SPI Signal

Step4. Choose the position to start the search by selecting one of the following:
 Start At: Ds T , A, B, C, etc.; End At: Dp, A, B, C, etc.. Then click Next or Previous to search it.

When Found: Choose a Bar to mark the result: A, B, C, etc..

- Step5. Click Statistics to show the number of instances of the search results.
- Note: It is available only when searching through a Bus.

Ceale: 3. 04120ns Total: 20. 48us			Pos:-10.15us A Pos:-10.15us → A - T = 10.15us → Range:-10.226032us ~ B Pos:150ns → B - T = 150ns →
Bux/Signal	Trigger	Filter	-10. 210826ur-10. 195619ur-10. 100419ur-10. 165206us -15 159s -10. 194794ur-10. 1
▼ Bus1			(0X01)(0X02)(0X03)(0X04)(0X05)(0X06)(0X07)(0X08)(0X09)(0X0A)(0
0A 0A			10ns 10ns 10ns 10ns 10ns 10ns 10ns 10ns
A1 A1			Tavefora-Find
● A2 A2			Activate the function of Chain-Data-Find
CA3 A3			eux/signal Nation:
• A4 A4			Busi Next Previous Close
of AS AS			Cas Rem: Find: Min Value: Max Value:
🥑 A6 A6			Dota 🖌 🗕 🔽 🛛 🕅
₫ 47 А7			Start At: End At: When Found: Statistics
# 80 80			Ds Dp A Statistics
e B1 B1			Address: -1015 64
🥑 B2 82			
	-		

Fig 3-128: The A Bar is placed at the 0X08 of Bus1 where the condition of the Waveform-Find is set. The Statistic of Waveform-Find shows a "64".

Scale:2.3576ns Total:20.48us			Post=9.97us A Post=9.97us ↓ A - T = 9.97us ↓ ↓ A samet=10.02094us ~ B Post150ns ↓ ↓
Bus/Signal	Trigger	Filter	-10.017152u=10.005364us=9.993576us=9.981780us -9.977us -9.958212us=9.946424u
▼ Bus1			0X14 (0X15 (0X16 (0X17 (0X18 (0X19 (0X1A (0X1B (0X1C)
AD AD			10ns 10ns 10ns 10ns 10ns 10ns 10ns 10ns
A1 A1			20 Tavefors-Find X 20
● A2 A2			Activate the function of Chain-Data-Find
A3 A3			Dus/Tigral Name-
. A4 A4			Busi
🝼 AS AS			Bus Item: Find: Min Value: Max Value:
🥑 A6 A6			Data - IA FF
# AZ AZ			Start At: End At: When Found: Statistics
# 80 80			De V Do V A V Statistics
# 81 81			Address: -997 64
∉ 82 82			20. 48us

Fig 3-129: The A Bar is placed at the 0X1A of Bus1 where the condition of the Waveform-Find is set.

Scale: 5, 6539625 Total: 32768		Display Pos:0 A Pos:104 ▼ A - T = 104 ▼ Display Range:-141 ~ 143 B Pos:0 ▼ B - T = 1 ▼
Bus/Signal	Trigger	Filter -113.079-84.809 -56.54 -28.27 28.27 56.54 84.809 113.
Bus (SPI)	·	
● A0 A0	х	
●A1 A1	X	
A2 A2		
<mark>⊂ A3</mark> A3		Taveform-Find
6 A4 A4		Activate the function of Chain-Data-Find Bost/Signal Name:
45 A5		Eust Vext Previous Close
🥑 A6 A6		Eus Item: Find: Min Value: Max Value:
✓ A7 A7		
60 B0		Start At: End At: When Found: Statistics
e B1 B1		Address: 0
∉ B2 B2		
🥑 B3 B3		
6 84 84		

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Fig 3-130: The B Bar is placed at the 0X12 of Data of Protocol Analyzer SPI where the condition of the Waveform-Find is set.



3.3 Statistics Feature

Section 3.3 presents detailed information on the **Statistics** feature in the software interface. The **Statistics** feature presents user information pertaining to nine periodicities: **Full Period**, **Positive Period**, **Negative Period**, **Conditional Full Period**, **Conditional Positive Period**, **Conditional Negative Period**, **Start Pos**, **End Pos** and **Selected Data**.

Click on the Statistics icon 🛗, and an interface like Fig 3-131 or Fig 3-132 will appear.

Channel Selection Column Selection Condition Parameter Warning Parameter Refresh 🗖 Statistics Filter										
CHANNEL	Full Period	Positive Per	Negative P	Conditional	Conditional	Conditional	Start Pos	End Pos	Selected Data	
AO	211	212	211	0	0	0	Ds	Dp		
A1	52	53	52	0	0	0	Ds	Dp		
A2	0	0	1	0	0	0	Ds	Dp		
A3	0	0	1	0	0	0	Ds	Dp		
A4	0	0	1	0	0	0	Ds	Dp		
A5	0	0	1	0	0	0	Ds	Dp		
A6	0	0	1	0	0	0	Ds	Dp		
A7	0	0	1	0	0	0	Ds	Dp		
B0	0	0	1	0	0	0	Ds	Dp		
B1	0	0	1	0	0	0	Ds	Dp		•

	C. CONTRACTOR	Quin Tank	States 1	**		54012 +	-		e Pasa I	• Court 1	الم الم
10 25 4 5	00	- 2.59	1224ur v 143,1436 nga 77 368	# 12 [20]		M	1	5 ** Haig T + 52 5938+ T = 52 5924m	w 28 - 1	A H+ Eas + Comp-Rate 121.005	-1
Bullips	Trigger	12-		15	-10		1	3	M) 53	e	. 2.
But DID	in the	10.0	17.00	DATA D	d1 / /	DATA D		DATA D	and the second	MATA DIST	1
# A2 - 11	x	0 1	1111	11111	0.0.0.0	11111	1111	11111	1000000	ALIALA	-
**1 10	16 -	10	П			Π					
# A2 A2	1.001	1.00									
e 45 11	1.82	-0									
# AK		10.1									
* 41 Al	1963	1.00									
# M 10	IN.	100									
# 43 M		18									
***	1.98	1.00									
# BC 10	1186.00	1									
		2.000									
# 12.11											
	1.81	1.18									
	(H)		1						1		
enel Sebelari Cal				ng Paramiter	(Refrect)	1" 3406078			1		
enal Selectors Cal	elui el	Canaltan Par Inte Fer Life	and the state	On Room	Control	Conditional	Ret for	Inter			
and Selected		Candillan Par	andra Via atra T	Orothord	Constrant.	Conditional	Dist for	0p 0p	J [Seesterperal]		
end Selector. Cal MHDCut/en	el. el.	Candilian Par Inte Fer Line 21	antin Via atra T	Centrone	Constrant.	Canditonal	Dat for Dr Dr Dr Dr Dr	Up Up Up Up	J [DemostOria]		
end Selector. Cal MHDCut/en	el. el.	Candilian Par Inte Fer Line 21	antes Va atra t	Croftson	Constrant.	Canditonal	Diat Pro Do Do Do Do Do Do Do Do	Up to	J DescherDeta	-	
end Selector. Cal MHDCut/en	et. 4 en belefter nit For 50 e	Candilian Par Inte Fer Line 21		Circlined 0 0 0 0 0 0 0 0 0	Continue	Conditional	Diat Pro	00 00 00 00 00 00	L [beneroes]		
enal Salettar WebCi Fulder 0 0 0 0	et. 4 en belefter nit For 50 e	Candition Pro-		Circlined 0 0 0 0 0 0	Constrant.	Canditonal	Diat Pro Do Do Do Do Do Do Do Do	Dp Dp Dp Dp Dp Dp	J Dember Data		2

Fig 3-131: Statistics table

Fig 3-132: Logic Analyzer with Statistics Enabled

There are four options for adjusting how statistical information may be presented. These four options are **Channel** Selection, Column Selection, Condition Parameter and Warning Parameter.

Channel Selection

erert S	elec	-			-			
	\hat{T}		5		0	÷.	I.	0
lot A	P	Þ	P	P	17	P	P	P
WE.	P.	P	P	P	12	P	P	P
w.C	F	P	P	P	P		P	P
utD	F	17	17	г	17	17	-	г
OTE	-	r	E.	Π.	r.	Π.	Π.	Г
wt.F	1	17	1	П	17	17	Г	г
wi d	r.	-	Г.	r,	Π	17	Π.	Γ.
WE H	E.	F	Ŧ.	1	17	F	-	F
ut1	E.	۳.	г	17	1-	Γ.	Π.	r
at J	-	17	17	П	г	17	1	5
WER.	г	r	F	г	17	1	Г	г
HTL:	٣	F	٣	-	r	17	17	г
ut.H	г	r	F	г	17	Γ.	П	Γ.
or.N	r	T	П	Г	r	F	Γ.	r
ut.o	F	17	17	-	E	1	-	5
	17	t	E	Г	r.	F	1	r

Fig 3-133: **Channel Selection**. Allow the choice of pins in which port will be included in the statistical analysis of a test run.



Column Selection

Column Selection	×
Probe	
▼ Full Period	
🔽 Positive Period	
🔽 Negative Period	
Conditional Full Period	
🔽 Conditional Positive Period	
🔽 Conditional Negative Period	
🔽 Start Pos	
🔽 End Pos	
🔽 Selected Data	
OK Cancel	

Fig 3-134: **Column Selection**. Allow the choice of items which will be considered in the statistical results.

Condition Parameter

Condition Parameter	×
Conditional Full Period	
400ns <= Time <=	= 400ns
Conditional Positive Period	
200ns <= Time <=	= 200ns
Conditional Negative Period	
200ns <= Time <=	= 200ns
ОК	Cancel

Fig 3-135: **Condition Parameter.** Allow the setting of time intervals for Conditional Full Period, Conditional Positive Period and Conditional Negative Period.

CHANNEL	Full Period	Positive Per	Negative P	Conditional	Conditional	Conditional	Start Pos	End Pos	Selected Data	
A0	211	212	211	0	0	0	Ds	Dp		
41	52	53	52	0	0	0	Ds	Dp		
42	0	0	1	0	0	0	Ds	Dp		
A3	0	0	1	0	0	0	Ds	Dp		
A4	0	0	1	0	0	0	Ds	Dp		
A5	0	0	1	0	0	0	Ds	Dp		
A6	0	0	1	0	0	0	Ds	Dp		
A7	0	0	1	0	0	0	Ds	Dp		
B0	0	0	1	0	0	0	Ds	Dp		
B1	0	0	1	0	0	0	Ds	Dp		

Fig 3-136: The Numbers of Data Qualified by Condition Parameter



Warning Parameter

Warning Parame	ter	x
🔽 Activate Warn	ing Setting	
Conditions	Min	Max
Period	✓ 10us	🔽 100us
C Frequency	□ 10KHz	100KHz
	ОК	Cancel

Fig 3-137: Warning Parameter. Set the conditions which will be marked to call users' attention.

Channel S	Selection Column Se	election Condition	Parameter Wa	arning Parameter	Refresh	Statistics Filte	r			
CHANNEL	Full Period	Positive Per	Negative P	Conditional	Conditional	Conditional	Start Pos	End Pos	Selected Data	
A0	211	212	211	0	0	0	Ds	Dp		
A1	52	53	52	0	0	0	Ds	Dp		
A2	0	0	1	0	0	0	Ds	Dp		
A3	0	0	1	0	0	0	Ds	Dp		
A4	0	0	1	0	0	0	Ds	Dp		
A5	0	0	1	0	0	0	Ds	Dp		
A6	0	0	1	0	0	0	Ds	Dp		
A7	0	0	1	0	0	0	Ds	Dp		
BO	0	0	1	0	0	0	Ds	Dp		
B1	0	0	1	0	0	0	Ds	Dp		-

Fig 3-138: The numbers of data qualified by warning conditions are printed in black, otherwise in red.

3.4 Customize Interface

Section 3.4 presents detailed instructions pertaining to how to **modify** the **Waveform Display Mode**, how to **modify** the **Ruler Mode**, how to **modify** the **Waveform Height**, and how to **modify** the **Correlated Setting**.

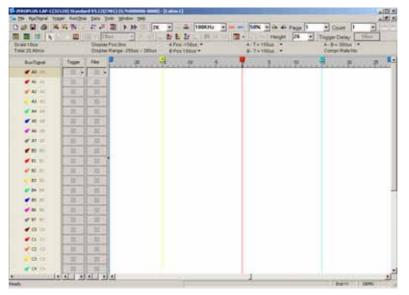


Fig 3-139: The Interface Layout Shown in Default Settings



3.4.1 Modify Waveform Display Mode

To modify the display mode, users can use icons on the tool bar/box, or menu. For the menu, go to **Tools** and click **Customize**. See *Fig.3-14*0

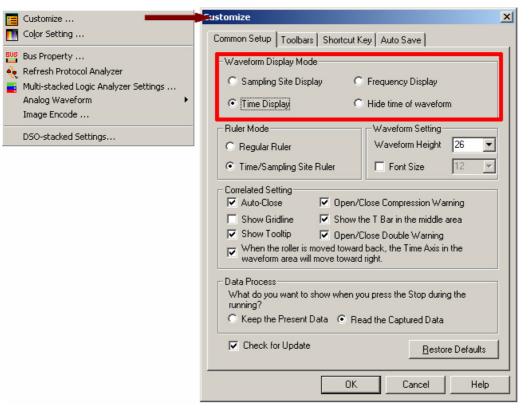


Fig 3-140: Customize the Display Mode by Using the Tool Bar



Fig 3-141: Tool Bar

Waveform Display Mode – There are four display modes to determine the method of capturing data from sampling: Sampling Site Display, Time Display, Frequency Display and Hide time of waveform.



3.4.2 Modify Ruler Mode

Use the menu to modify the Ruler Mode.

Go to Tools and click Customize. See Fig. 3-142

Customize	stomize 🛛 🕹									
Common Setup Toolbars Shortc	ut Key Auto Save									
Waveform Display Mode										
C Sampling Site Display	C Frequency Display									
C Time Display	Hide time of waveform									
- Ruler Mode	Waveform Setting									
C Regular Ruler	Waveform Height 22 💌									
Time/Sampling Site Ruler	Font Size 12									

Fig 3-142: Ruler Mode

Regular Ruler



Fig 3-143: Scales in Regular Ruler

Time/Sampling Site Ruler



Fig 3-144: Scales in Time/Sampling Site Ruler

Ruler Mode – There are two styles of Ruler: (Regular Ruler, Time/Sampling Site Ruler) **Regular Ruler:**

Presented in increments of 5.

Time/Sampling Site Ruler (default):

Presented in increments of 25ns.



3.4.3 Modify Waveform Height & Correlated Setting

To modify Waveform Height, click **Tools → Customize**.

Waveform Height

Set the height of waveform (18-100) in chosen items at toolbar that will show the amplitude of the waveform.

ustomize								
Common Setup Toolbars Shortcut H	Key Auto Save							
Waveform Display Mode								
C Sampling Site Display	Frequency Display							
C Time Display @	Hide time of waveform							
Ruler Mode	Waveform Setting							
C Regular Ruler	Waveform Height 22 💌							
• Time/Sampling Site Ruler	Font Size 12							

Fig 3-145: Waveform Height

Waveform Height = 18

				Property and a second s	10.000	1.000	استال با
				* **	1		
hafips	(married by the second	1 ter		# AL /-			
100		-	HARD	440-0	1		
#2 +1.	EEE			KA8.30	101	1	
1.5				* Are	(10)	81	
				# 48, 10.	(#)	1	1
		-1-		***-	181	-	
		-			1.013	(11)	
2							
12 12				· ** **		3	
	1	-			10	81	
R10 - 1				< 80 T	(M)	-71	
-		40	4	2 14 24	1	3	
F	-ig 3-1	40-	I	г		116	2

Fig 3-146-2

Waveform Height = 40

Fig 3-146: Examples of Waveform Height

Correlated Setting

Select Auto-Close in the following figure.

Correlated Setting	🔲 Open/Close Compr	ession Warning							
🔲 Show Gridline	🔽 Show the T Bar in t	he middle area							
🔽 Show Tooltip	🔽 Open/Close Double								
When the roller is moved toward back, the Time Axis in the waveform area will move toward right.									
Data Process What do you want to show when you press the Stop during the running?									
 Keep the Present Data Read the Captured Data Check for Update <u>R</u>estore Defaults 									
	ОКС	Cancel Help							

Fig 3-147: Correlated Setting

Bus/Signal	Trigger	Filter	-25ns -
🥑 AO AO	•	•	
🥑 A1 A1			
🥑 A2 A2			
🥑 A3 A3			
🥑 A4 A4			
🥑 A5 A5			
🥑 A6 A6			
✓ A7 A7			
🥑 BO BO			
🥑 B1 B1			

Bus/Signal	Trigger	Filter	25ns -18.75n
🥑 AO AO	•	-	
🝼 A1 A1			
🥑 A2 A2			
🧹 A3 A3			
🥑 A4 A4			
🧹 A5 A5			
🥑 A6 A6			
✓ A7 A7			
🥑 BO BO			
🥑 B1 B1			

Fig 3-148: An Example for Auto-Close

Auto-Close - With the cursor in the channel, when users try to drag a Bar, the Bar will stop at the approaching edge of the channel (Rising Edge or Falling Edge).

Tip: In the above example, when dragging the C Bar, the A Bar will stop at the Raising Edge of A1.



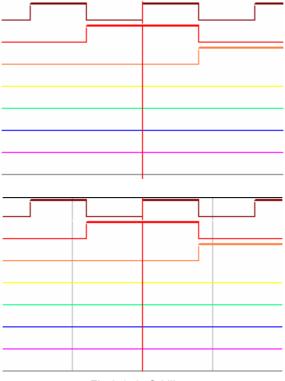


Fig 3-149: Gridlines

Show Gridline - The gridlines will be displayed on the waveform area.

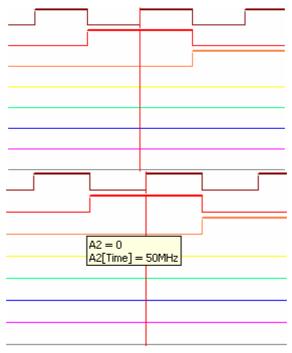


Fig 3-150 - Tooltips

Show Tooltip – Leave the mouse over a waveform and the description will be shown.

Show the T Bar in the middle area -Show the T Bar in the middle of the Waveform Display Area after triggering. When the roller is moved toward back, the Time Axis in the waveform area will move toward right-

When the option is selected and users move the roller in the middle of Mouse directly toward back, the scrollbar will move toward right correspondingly.

Check for Update: The Logic Analyzer software will automatically check for updates when being started. **Restore Defaults:** The Waveform Display Mode, Ruler Mode, Waveform Setting, Correlated Setting and Data Process will return to the default setting.



3.5 Auto Save

To save the captured data for a long time, users can use icons on the tool bar/box, or menu.

For the dialog box, go to **File** menu to click **Auto Save** or go to **Tools** menu to select **Customize** and select **Auto Save**. See *Fig 3-151*.

	New	Ctrl+N
Ż	Open	Ctrl+O
	Close	Ctrl+F4
	Save	Ctrl+S
	Save As	
•	Auto Save	
6	Export Waveform	Ctrl+Shift+E
(Export Packet List	
Ô	Capture Window	Ctrl+C
	Language	•
5	Print	Ctrl+P
	Print Preview	
	Recent File	
	Exit	

mmon Setup Toolba	rs Shortcut Key	Auto Seve
V Activate		
ile Hune: LA		
Save Fath		
C:\Documents and Se	ttings\Administr	ator\#y
Repetitive Run Time Interval:	Duta Display Mer Every Esneve Open the fir stopping the	d rst file after
		Default

Fig 3-151-1: Auto Save on File Menu

Fig 3-151-2: Auto Save Item of Customize

Fig 3-151: Auto Save

Auto Save: The default is not activated; after activating, it keeps working and users also can choose Cancel to close it.

Activate: The default is not activated: after activating, it keeps active and users also can choose **Cancel** to close it. **File Name**: Before users name the file, the file name is defaulted as LA. In fact, the saved file name can add a serial number for the file automatically.

Save Path Name: Users can enter the path directly or choose the path from the selected path button

Time Interval: When the auto save function is activated, the time interval from one finished sampling to the next activated sampling can be set according to users' requirements; the default is 1s, and the unit can be selected from s(second), m(minute) and hr(hour).

Every Renewal: When the repetitive run is activated, the waveform image or the state image will renew again and again.

Open the first file after stopping the Run: When the repetitive run function is activated, the waveform only displays the first file and it isn't renewed; when the repetitive run is stopped, the waveform still displays the first file.



Fig3-152: Auto Save



3.6 Color Setting

To modify Color, click **Tools → Color Setting**

lor Setting Workaround Waveform			ļ
Name	Relating	Color	_
Waveform Background List Background 1 List Background 2 Cursor Grid Unknown Line Default Bus Bus Text List Text Time Text Bus Error Bus Error Bus Error Bus Error Text Singnal Filter Rar			
Preview 0 1 0 10 10 10 10	0 0 0	 automatically according to ratio. 	esponding color changes the contrast
	Cano	background	is white.

Fig 3-153: Workaround and Waveform Color Setting

Workaround - Set the workaround color of the Logic Analyzer and the text.

orkaround Waveform			
Name	🗖 Relating	Color	
Waveform Background			
List Background 1			
List Background 2			
Cursor			
Grid			
Unknown Line			
Default Bus			
Bus Text			
List Text			
Time Text			
Bus Error			
Bus Error Text			

Fig 3-154: Workaround Color Interface

Waveform Background: The Logic Analyzer's Waveform Viewer Background Color.

List Background 1: The Logic Analyzer's First Listing Viewer Background Color.

List Background 2: The Logic Analyzer's Second Listing Viewer Background Color.

All optional items include the current color of Cursors, Grid, Unknown Line, Default Bus, Bus Text, List Text and Time Text (users can scroll the vertical wheel to view the selectable items).

Bus Error: Users can configure the color of Bus Error Data from the Color Setting dialog box.

Bus Error Text: Users can configure the color of Bus Error Text from the Color Setting dialog box.

Signal Filter Bar: Users can configure the color of Signal Filter Bar from the Color Setting dialog box.

Relating: When users select one item to change the color of the item, and users want to change other items into

the same color, they can select other items at the same time in the Relating column, then the selected items will

be changed into the same color. So it is convenient for users to change many items into the same color once.

After the background is altered, corresponding color automatically changes according to the contrast ratio: When users set the color for the workaround and select the option, the system will switch other colors automatically to become the contrast color.



When being printed, the background is white: When being printed, the background color is white.

Name	🗌 🗖 Relating	Color	Linewidth 🔄
AO			1 pixel
A1			1 pixel
A2			1 pixel
A3			1 pixel
Α4			1 pixel
A5			1 pixel –
A6			1 pixel
A7			1 pixel
BO			1 pixel
B1			1 pixel
B2			1 pixel
B3			1 pixel
B4			1 pixel
B5			1 pixel
R6			I 1 nivel I
	<u> </u>		
1010			

Waveform - Change the color of the Buses or signals on the waveform area.

Fig 3-155: Waveform Color Interface

Waveform: The channel color can be varied by users.

Linewidth: The linewidth can be adjusted by the users' requirements; there are three options which are 1pixel, 2 pixel and 3 pixel.



3.6.1 Modify Workaround Color

To modify the workaround color, click the color block shown in Fig 3-154. A **Color** panel, shown in Fig 3-156, will appear. Select a color shown on the panel or click on **Define Custom Colors** to create the desired color.

Color	? ×
Basic colors:	
<u>C</u> ustom colors:	
	Hu <u>e</u> : 160 <u>R</u> ed: 0
	<u>S</u> at: 0 <u>G</u> reen: 0
Define Custom Colors >>	Color Solid Lum: 0 Blue: 0
OK Cancel	Add to Custom Colors

Fig 3-156: Color Panel with Its Advanced View



3.6.2 Modify Waveform Color

Foreground color refers to the color of the output signal lines in the Waveform Display Area. *Fig3-157* presents how to change colors of a signal or some signals. Repeat the following procedures if users need to change colors of many signals.

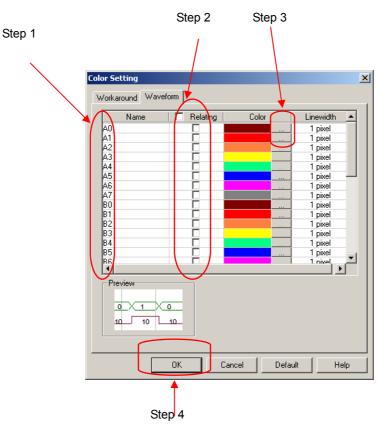


Fig 3-157: Stepwise Illustration of Changing Waveform Colors

- Step 1: Select several Optional Items.
- Step 2: Select the corresponding items in the relating.
- Step 3: Choose a color by following the method shown in Fig 3-157.

Step 4: Click OK to change their colors into the same, for example A1, A2, A3 and A4.

Here is a sample of an altered Logic Analyzer software interface which will be used for further demonstrations in subsequent chapters. See *Fig 3-158*.



The second se	S.N.	and a state of the	5 30 TH	- 4 1000	Hu - H	and the statement of the statement of the statement	26 · Topp	er Deney 111	
Down 10um Tyrie 30 Admin		Display Fox Display Flat	(8+4 gm-25044 - 29044	A Pos-150us * B Pos 150us *		A-T+15048. * &-T+15048. *		ran Flate No	
Bulipe	1 frager	The E	- united and	4		and the second	12	and the second	3. 1
# AL	11.4		THMM		11 1				
# AL -15	1111	=							
* 42 M	1001	1.96.1	11007	1000	A CONTRACTOR OF A CONTRACTOR OF A CONTRACTOR OF A CONTRACTOR A CONTRAC				
44.11	1.18.11	1083							
* A4 21	28.	22							_
· · · · ·		111		-					
6 M	58.1	ALC: NO.			_				
# 10 at	100	12		_	_				
e m	100.00	112801							
e 11 m	100	11 1							
4 M. H.	1 11 1	1 m							
	22.	22							
ar 24 11	100	1 H							1
	1.00.11	C.H.							
100	100	1.32		-					
er 10 -	1000	21				111			
100	100	100							
e o. 11	11.	1282							_
100	100	35							_
0.01	100	T							
100	10mc	Long of							
er under er e						1		be be	

Fig 3-158: An Altered Interface Sample to Be Used in Subsequent Chapters



3.7 The Flow of Software Operation

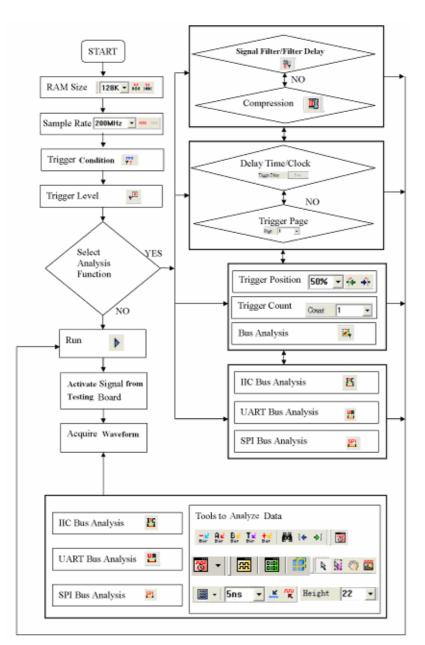


Fig 3-159: Software Flow Diagram

Conclusion

Information demonstrated in this chapter is only for entrance level. There are more advanced approaches which may require fewer steps than those shown in this chapter. This chapter is meant to equip users with sufficient grounding of the Logic Analyzer's software interface.



4 Introduction to Logic Analysis

- 4.1 Logic Analysis
- 4.2 Bus Logic Analysis
- 4.3 Plug Analysis
- 4.4 Bus Packet List
- 4.5 Bus Analysis
- 4.6 Compression
- 4.7 Signal Filter and Filter Delay
- 4.8 Noise Filter
- 4.9 Data Contrast
- 4.10 Refresh Protocol Analyzer
- 4.11 Memory Analyzer
- 4.12 Multi-stacked Logic Analyzer Settings
- 4.13 DSO-stacked Settings



Objective

Chapter 4 gives detailed instructions on performing two basic analysis operations and other advanced analysis applications with the Logic Analyzer. These two basic analysis operations are the Logic Analysis and the Bus Logic Analysis, which are fundamental to all further applications. The other advanced analysis applications are the I2C (Inter Integrated Circuit) Analysis, the UART (Universal Asynchronous Receiver Transmitter) Analysis, the SPI (Synchronous Peripheral Interface) Analysis, Compression, Signal Filter Setup, Filter Delay Setup, etc..

4.1 Logic Analysis

Logic Analysis is meant for a single signal analysis. Section 4.1 gives detailed instructions on the software's basic setup.

Basic Software Setup of the Logic Analysis

Task 1. Clock Source (Frequency) and RAM Size Setup

Step1. Click icon or click Sampling Setup from Bus/Signal on the menu bar, the dialog box as shown in Fig 4-1 will appear.

<u>. M</u>	Sampling Setup	Sampling Setup
	Channels Setup Signal Filter Setup	Clock Source Asynchronous Clock
	Group into BusCtrl+GUngroup from BusCtrl+U	Synchronous Clock C External Clock G Rising Edge Frequency: 1000Hz
	Expand Collapse	C Falling Edge (Min:0.001Hz, Max:100MHz) Note: The external clock voltage level is the same as the port A trigger level
	Format Row Rename	Sampling Signal Filter RAM Size ZK T Data Compression Signal Filter Signal Filter Signal Filter
		Apply OK Cancel Restore Defaults Help

Fig 4-1 - Clock Source

Step 2. Clock Source (Frequency) Setup

Internal Clock (Asynchronous Clock)

Click on **Internal Clock**, and then select the Frequency from the pull-down menu to set up the frequency of the device under test (DUT). The frequency of the Internal Clock must be at least four times higher than the frequency of the Oscillator on the DUT. Or, select the frequency from the pull-down menu on Tool Bar as Fig 4-2 shows.

Tip: Connect the output pin of the oscillator from the tested board to the signal connector of the Logic Analyzer to measure it by using the internal clock of the Logic Analyzer.

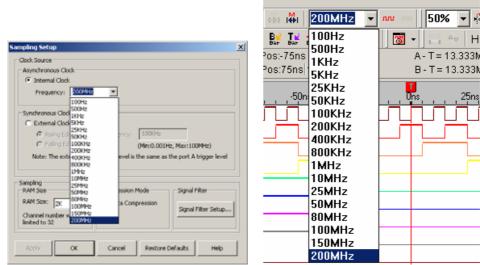


Fig 4-2 - Clock Source Pull-down Menu

External Clock (Synchronous Clock)

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Zeroplus Technology Co., Ltd.

Click on **External Clock**, and then select "Rising Edge" or "Falling Edge" as the trigger condition of the DUT. In the Frequency column, type the frequency of the oscillator on the DUT.

Tip: The External Clock is applied when the frequency of the oscillator on the tested board is exceeds the range of the internal clock of the Logic Analyzer. Connect the output pin of the oscillator on the tested board to the CLK pin of the Logic Analyzer.

Step 3. RAM Size Setup

Click the RAM Size received or from the pull-down menu in the Sampling Setup dialog box as shown in Fig 4-3.

	128K 🔻	M M 441 4 4	RAM Size		© Exter © R C F Note:	manda and a second a se	2)
ĸ	2K 16K 32K	B¥ T¥ Bar Ios:-75ns	Channel nur ² limited to 32 ¹	28K 🔽 K 6K 2K	Sampling RAM Size _	Dan't show me this warning again. CK 256K Data Compression	jer level
17	64K 128K 256K	Pos:75ns 50r	6	4K 28K 56K		Jinber will be	Help

Fig 4-3 – RAM Size

Tips 1: The Double Mode is available for the Modules in Table 4-1 except for the LAP-C(16032),

LAP-C(16064) Modules.

2: The relationship between RAM Size, Signal Filter Mode, Compression Mode and Channels as shown in Table 4-1 and Fig 4-3.

Status		Normal Mode			Double Mode		
Model No.	RAM Size/ Channels	Channels Available	Compression Mode & Signal Filter Mode	RAM Size/ Channel s	Channels Available	Compression Mode & Signal Filter Mode	
LAP-16032U	2K ~ 32K	16 channels	Available	64K	16 channels	Disable	
LAP-16064U	2K ~ 64K	16 channels	Available	128K	16 channels	Disable	
LAP-16128U	2K ~ 128K	16 channels	Available	256K	16 channels	Disable	



LAP-32128U-A	2K ~ 128K	32 channels	Available	256K	16 channels	Disable
LAP-321000U-A	2K ~ 1M	32 channels	Available	2M	16 channels	Disable
LAP-322000U-A	2K ~ 2M	32 channels	Available	4M	16 channels	Disable
LAP-C(16032)	2K ~ 32K	16 channels	Available	-	-	-
LAP-C(16064)	2K ~ 64K	16 channels	Available	-	-	-
LAP-C(16128)	2K ~ 128K	16 channels	Available	256K	16 channels	Disable
LAP-C(162000)	2K ~ 2M	16 channels	Available	4M	16 channels	Disable
LAP-C(32128)	2K ~ 128K	32 channels	Available	256K	16 channels	Disable
LAP-C(321000)	2K ~ 1M	32 channels	Available	2M	16 channels	Disable
LAP-C(322000)	2K ~ 2M	32 channels	Available	4M	16 channels	Disable

Task 2. Trigger Property

	Due Triegen Celue	Trigger Property	×
	Bus Trigger Setup	Trigger Content Trigger Delay Trigger Range	
ŤΤ	Channel Trigger Setup		1
ų 🏽	Trigger Property	Trigger Count Post A	
i.	Trigger Mark	CMOS(SV) 25 (V)	
÷.	Pulse Width Trigger Module(Option)	Port B (Min:1, Max:65535)	
14		TTL 15 (V)	
\boxtimes	Don't Care	Port C	
		TTL 1.5 M	
	High	Port D	
	Low	TTL 1.5 M	
Z	Rising Edge		
50	Falling Edge		
	Either Edge		
PAN -	contra cago		
	Reset	OK Cancel Default Help	

Fig 4-4 - Trigger Property

Step2. Trigger Level Setup

Click the pull-down menu of **Trigger Level** on Port A, B, C and D to select the Trigger Level as the voltage level that a trigger source signal must reach before the trigger circuit initiates a sweep.

Tip: There are four commonly used preset voltages for Trigger Level, TTL, CMOS (5V), CMOS (3.3V), and ECL. Users also can define their own voltage from -6.0V to 6.0V to fit with their DUT, if the number users define is not in the range, the Fig 4.5 dialogue box will appear.

Port A represents the pins from A0 ~ A7 on the signal connector of the Logic Analyzer, and so do Port B, C and D. The voltage of each port can be configured independently.

Step1. Click icon or click Trigger Property from the Trigger on the Menu Bar. The dialog box will appear as shown in Fig 4-4.



Trigger Property	x
Trigger Content Trigger Delay Trigger Range	
Trigger Level Trigger Count Port A 1 CM0S(5V) 2.5 Port B ZEROPLUS Logic Analyzer TTL Port C Port D OK User Defi OK	
OK Cancel Default Help	

Fig 4-5 – Trigger Level Error

Step3. Trigger Count.

Type the numbers or select the number from the pull-down menu of the Count **Count T** on the Tool Bar or click the pull-down menu of the **Trigger Count** on the Trigger Property dialog box as shown in Fig 4-6. The system will be triggered at the position where the Trigger Count is set as shown in Figs 4-6, 4-7 and Fig 4-8.

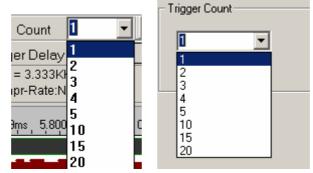


Fig 4-6 – Trigger Count Pull-down Menu

Cole II an A		III - 4.42	Image: 10 Image: 10 <thimage: 10<="" th=""> Image: 10 <thimage: 10<="" th=""> Image: 10 <th< th=""></th<></thimage:></thimage:>
bu/ligal	Triger	Tiller	•
· 40	1.	- 55 -	
★A1 11	11:06.01	111	
1 A 40	100	96	
. AB AL	1186.5	- 38-	
a 44 m	100	1.00	
# 45 .45	1	18	
***.AL	100	1.100	
8 K 10	1.000	1.00	
# 80 10	06	10	

Fig 4-7 – Trigger Count Screen Shot 1



	· · ·	TT T	ta Leila Biele Bie B b bb 120K + 36 4 100MHz + 4 10 10K + 4 4 5 242 1 + Cast 5 - 347564- 3 2 5 1 25 2 4 4 4 4 1 + 5 1 5 1 20 - Triger 144 - 1 + 1 5 100 - Tet & LUILine & A fet - 12 5 5 4 - 2 + 1 5 1000 - Set 5 - 2 - 2 5 1000 - A fet - 12 5 5 4 - 2 + 1 5 1000 - Set 5 - 2 - 2 - 2 5 1000 - B fet 6 - 2 - 2 - 2 5 1000 - B fet 6 - 2 - 2 - 2 5 1000 - B fet 6 - 2 - 2 - 2 5 1000 - B fet 6 - 2 - 2 - 2 5 1000 - B fet 6 - 2 - 2 - 2 5 1000 - B fet 6 - 2 - 2 - 2 5 1000 - B fet 6 - 2 - 2 - 2 5 1000 - B fet 6 - 2 - 2 - 2 5 1000 - B fet 6 - 2 - 2 - 2 5 1000 - B fet 6 - 2 - 2 - 2 5 1000 - B fet 6 - 2 - 2 - 2 5 1000 - B fet 6 - 2 - 2 - 2 5 1000 - B fet 6 - 2 - 2 - 2 5 1000 - B fet 6 - 2 - 2 - 2 5 1000 - B fet 6 - 2 - 2 - 2 5 1000 - B fet 6 - 2 - 2 - 2 5 1000 - B fet 6 - 2 - 2 - 2 - 2 - 2 - 2 - 2 - 2 - 2 -
bu/lipsi-	Trigger	Filter	2
€ ME ==	5.	18%	
# AE 16	20	86	
≪.42 .4€	Date:	100	
- A3 50	Sat.	12	oen/
# 84 211	100	12	oen,
₹ 45.10	2417	55	aven
# H =	1 R.S	R	om,
600	Cast 1:	12	oen.
# 80 H	1.887	12	cen,

Fig 4-8 – Trigger Count Screen Shot 2

Step4. Trigger Page/ Delay Time and Clock

The Trigger Page and the Delay Time and Clock can't be applied at the same time.

1. Trigger Page:

Click **Trigger Page**, then type the numbers or select the numbers from the pull-down menu of the Page Page 1 • on the Tool Bar or click the pull-down menu of the Trigger Page on the "Trigger Delay" page of the Trigger Property dialog box as shown in Figs 4-9, 4-10 and 4-11. The selected page numbers will be displayed on the screen.

Tip: The Trigger Bar (T Bar) will not be displayed when the setup of the Trigger Page is more than 1.

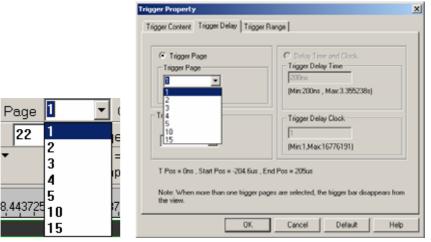
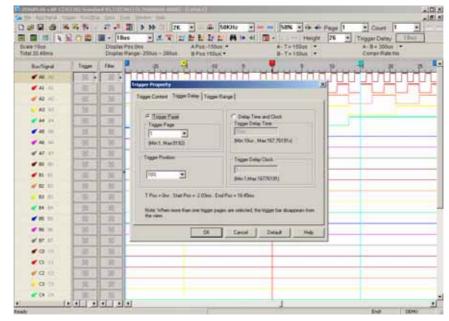


Fig 4-9 - Trigger Page





and and a second	k vi ti ki n di	Display P	· · · · · · · · · · · · · · · · · · ·	2 2 1 1 1+ 41 1 - Hangte 26 + Togs 5000 - A-T+15000 + A	Court 1 -
Bactignal	Tages	-Film		B	
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🖌 AL -11	-	- 70	Trigger Property		
🖉 AQ 11	100	36-	Tagge Canter Toppe Delay Ta	ger flange	
a ca	38	-41		lan and a second se	
at 24, 24	1.00		- Trave From Trave Proc	C Delle Ties and Dock	
2 40 m	16	11		Proc.	
* M ==	1000	100	(Hert Mar 2132)	. Min 15ke , Mac 197, 701 Maj	
4.47.67	1000	1.24	Tagge Paultin	Transmitter territory	
e 80 m	100	35		Trape Delay Club	
# BS 91	1000	- 34 - 1	100	(Arrow 1.04 as 1677(2101)	
# E 11	100	:81			
83 83	1.007.0	1.001	T Pas+live .21at Pas+7212b	a. Lod Pas + 100.27m	
ar 84 .04 "	- 16	-20	Note Suffeen many Part and Supp	e pages are conclud, the higgs has disappears have	
* # = -	100	10	fa ven		
# M	100.0	1.00.1	06	Canol Delait Hig	
¥ 87.11	10	12	2		
* G = 0	100	1288			
* 0 iii	187	38			
₹ @ 12		36			
- O D	12	37			
CR (1)	2	24			

Fig 4-10 – Trigger Page and Screen (1)

Fig 4-11 – Trigger Page and Screen (2)

2. Delay Time and Clock

Click the **Delay Time and Clock**, then type the numbers into the column of the Trigger Delay Time or type numbers into the Trigger Delay Clock at the "Trigger Delay" page of the Trigger Property dialog box as shown in Fig 4-11. Or type the numbers into the column of Trigger Delay Trigger Delay 200ns on the Tool Bar. The system will display the Start of the waveform.

- **Tip:** The formula of Delay Time and Clock is "Trigger Delay Time = Trigger Delay Clock * (1/ Frequency)". To use the compression mode, the < Delay Time and Clock > will be unavailable.
- Step5. Trigger Position Setup

Type the percentages or select the percentages from the pull-down menu of the Bar or click the pull-down menu of the Trigger Position on the "Trigger Delay" page of the Trigger Property dialog box as shown in Figs 4-12, 4-13, 4-14, and 4-15. The selected Trigger Position percentages will be displayed on the right side of the screen of the system.

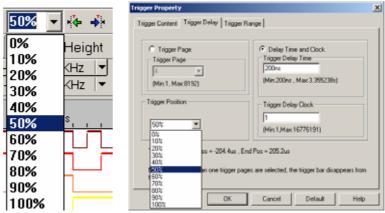


Fig 4-12 - Trigger Position Pull-down Menu



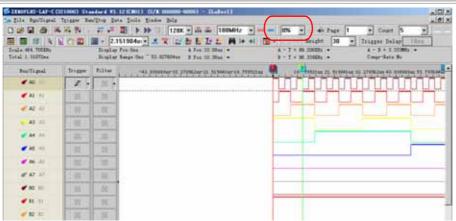


Fig 4-13 – Trigger Position 0%

	Tereen Bu	Tripler	LETERIUL: Off Score Score Local - (Letter) (101) a Totle Unite Big (101) a Totle Unite Big (101) b bb (121) T Tatk with an Internet Big (100) S1004w at the state Big (100) S104w at the state Big (100) S1004w at the state Big (100) S104w at the state Big (100) S1004w at the state Big
buffiged.	Triger	Tiller	· · · · · · · · · · · · · · · · · · ·
* A2 10	1.	100	
≪ AI 10	1186	H	Distance,
₹ 42 Al	1.49.70		Dakasen
- A3 AL	1.000	- 10-	Dilzon
a 44 m	100	1	Unknown
2 45 -41	11	18	Unknown
· 14. 11	100	1	Unknown,
0 N V	1.48.70	1.001	Unknown,
# 80 10	06	10	Unknown
* 88 10		10	lhknom
* 1 10	3	12	Unknown

Fig 4-14 – Trigger Position 10%

2 25 2 2 2 3 3 3 2 25 2 3 4 4 5 2 24 4 5 5 4 2 24 4 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5		III - 2.	Image - 51 Image -	
In/light	Triger	Tilter	🔟 🐘 141. prosensor 18. promotov 18. na saartovr (n. 1799) na 🖳 🛛 18. frankrad 28. frankrad 18. prosensod 18. prosensod 18.	10000
# AD 10	1.	1000		П
	1186	H.	Linknown,	
1 42 A	1.00		linknoen	-
- AD	1.86.13	- 32	Unknown	
a 44 m	100	1.00	Unknown	-
	11	100	thingen	
· 16.10	100	1.100	Balansen	
000	1.000	1.00	Unknoem	_
# 80 HI	06	100	Unimosen,	
·	1.02	76	Uninovn	
	- 32		Unknown,	

Fig 4-15 – Trigger Position 70%

Step6. Trigger Range Setup

Click **Trigger Property** from the Trigger on the Menu Bar. Then, Click the Trigger Range, the dialog box will appear as shown in Fig4-16.

Tip: This function is mainly for the range control for the saved files after triggering. According to the procedures of the range control, users can start the save of data according to the requirement of its time and times to get the standard of data statistic status.



Trigger Property	×
Trigger Content Trigger Delay	Trigger Range
Range Setting	
Time Sample 💌	1 minute
	OK Cancel Default Help

Fig 4-16 - Trigger Range

1. Trigger Range: The default is not activated.

2. There are "Time Sample" and "Frequency Sample" in the part of Range Setting; the default is "Time Sample". The units of Time Sample are 'second', 'minute', 'hour' and 'day'. The unit of Frequency Sample is 'times'. Users can set the value by themselves in the editor box.

Task 3. Bus Trigger and Trigger Mark Setup

Step1. Click 🐺 icon or click Bus Trigger Setup and Trigger Mark from the Trigger on the Menu Bar. The menu is shown as Fig 4-17.

₩ ₩ ₩ ₩ ₩ ₩ ₩	Bus Trigger Setup Channel Trigger Setup Trigger Property Trigger Mark Pulse Width Trigger Module(Option)
	Don't Care High Low Rising Edge Falling Edge Either Edge
	Reset

Fig 4-17 - Trigger Menu

- Step2. Bus Trigger Setup
 - 1. Bus Trigger Setup



Bus Trigger			×
Bus Trigger Protocol A	nalyzer Trigger		
Bus Name	Operator	Value	
Bus1 👻	=	▼ 3F	
Data Format			
C Binary	O Decimal	O Decimal(Signed)	
Hexadecimal	O ASCII	🔿 Gray Code	
C Complement			
OK	Canc	el Default	Help

Fig 4-18 - Bus Trigger Dialog Box

Tip: The Bus Name item can be selected from the pull-down menu (It only displays the Bus name), and also the Decimal(signed), Gray Code and Complement Modes are added.

2. Protocol Analyzer Trigger Setup

Tip: This function can be used in the Modules, LAP-16032U, LAP-16064U, LAP-16128U, LAP-32128U-A LAP-321000U-A ,LAP-C(16032), LAP-C(16064), LAP-C(16128), LAP-C(162000), LAP-C(32128) and LAP-C(321000) after registering. And for the LAP-322000U-A and LAP-C(322000), it is not necessary to register as they can be used for free. Before registering, the button "OK" in the Protocol Analyzer Trigger dialog box is the button, "Register"; when users press this button, Register, a Register dialog box will pop up. Then users need to enter the correct Register Code so that they can use this function, Protocol Analyzer Trigger.

Bus Trigger Protocol Analyzer Trigger	
Allow Protocol Analyzer Trigger	
Protocol Analyzer: Protocol Packet: Value:	
Data Format	
C Decimal C Decimal(Signed)	
Hexadecimal ASCII	
🔿 Gray Code	
C Complement	
OK Cancel Default Help	

Fig 4-19-1 Before Registering

Register Dialog Box:

egister		×
The function is an optional p activate this function for you	urchased item.Welcome to pu ir necessary.	rchase its serial key to
Enter serial key:		
	ave questions about ordering w.Our sales team will respond	
>> By phone:	886-2-662022	225
>> Applications through Ema	ail: service_2@ze	eroplus.com.tw
>> Website:	http://www.z	roplus.com.tw
Conversion (C) 1007-2012-750	OPLUS TECHNOLOGY CO.,LTE	, .
Copyright(C) 1997-2012 2EK	.oreos recrimocodi co.,ere	υ.
		OK Cancel
ıs Trigger		X
Bus Trigger Protocol Ar	halyzer Trigger	
Allow Protocol An		
Protocol Analyzer:	Protocol Packet:	Value:
Bus1(I2C)	Start	0
	O ADDRESS	
	C Read	Data Format
	O Write	C Binary
	O A-ACK	C Decimal
	O A-NACK	C Decimal(Signed)
	O DATA	Hexadecimal
	O D-ACK	C ASCII
	O D-NACK	C Gray Code
	C Stop	C Gray Code
	C Stop	
	C Stop	

Fig 4-19 -2 After Registering

Allow Protocol Analyzer Trigger: When it is selected, the Protocol Analyzer Trigger function is activated. And then users can set Protocol Analyzer, Protocol Packet, Value and Data Format.

Protocol Analyzer: It only displays the name of Protocol Analyzer and only one name can be selected.

Protocol Packet: It is displayed according to the packet in every protocol analyzer.

Value: The value needs to be entered in the frame, and the data mode can be selected by users according to their requirements; the default is Hexadecimal! When a value can be input in the selected protocol analyzer data, the frame can be enabled! Or, the frame will be disabled! For example: Protocol Analyzer I2C, when the protocol packet is DATA, the frame can be used; to the contrary, when the protocol packet is START, the frame is disabled.

Data Format: The displayed value mode can be selected! There are five options: Binary, Decimal, Decimal(signed), Hexadecimal, ASCII, Gray Code and Complement.

Step3. Trigger Mark Setup

To find the item in the Bus better, users can activate the Trigger Mark function after starting Bus Trigger; the trigger mark is shown with T bar. According to the number of the trigger position, the T bar is displayed in order T0, T1, T2, T3, T4...and the color is red as the image below:

1. Bus: The trigger condition is "0"; the red T bar displays the trigger condition in order.



Bus/Signal	Trigger	Filter	P	0.667	3.567	5.667	67 14	667	10, 167	15.667	8, 167
▼ Bust	OE0 .	121 -	know (0X4)(0X	5 0X4	000	0001	X0) 0X4)(OXD)(OXC	X0X4)(0X5)(0X4	02
●A0 A	<u>=</u>	10									
●A1 A	-	8									
• A2 A		101									1
A 64 -	-	151									
		10									

Fig 4-20 - Bus Trigger Mark

2. Protocol Analyzer (I2C): The trigger condition is "Data=0"; the red T Bar displays the trigger condition in order.



Fig 4-21 - Protocol Analyzer Trigger Mark

Tip: The Trigger Mark function is available for the LAP-322000U-A, LAP-C(162000), LAP-C(322000) Modules, and it is not available for the LAP-16032U, LAP-16064U, LAP-16128U, LAP-32128U-A, LAP-321000U-A, LAP-C(16032), LAP-C(16064), LAP-C(16128), LAP-C(32128) and LAP-C(321000) Modules.

Task 4. Bus/Signal Trigger Condition Setup

Highlight a designated signal, and then set its required trigger condition.

- 1. Left click III to set the signal trigger condition as shown in Fig 4-22.
- 2. Right click is to set the signal trigger condition as shown in Fig 4-23.
- 3. Click **Trigger** on the Menu Bar and choose a trigger condition from the list of triggers as shown in Fig 4-24.

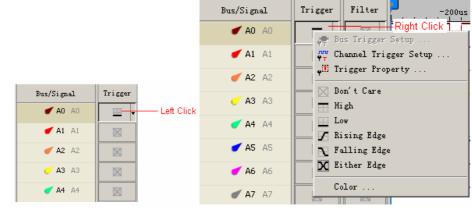


Fig 4-22 – Left Click on Trigger

Fig 4-23 - Right Click on Trigger



	Bus Trigger Setup Channel Trigger Setup Trigger Property
N	Don't Care High Low Rising Edge Falling Edge Either Edge
	Color

Fig 4-24 – Trigger Menu

Task 5. Run to Acquire Data

1. Single Run

Click the Single Run icon from the Tool Bar or press **START** button on the top of the Logic Analyzer (or press F5), then activate the signal from the DUT to the Logic Analyzer to acquire the data shown in the waveform display area.

2. Repetitive Run

Click the Repetitive Run is icon from the Tool Bar, then activate continuous signal to the Logic Analyzer to acquire the repetitive data, and then click the Stop icon to end the repetitive run.

Tip: Click 📓 icon to view all the data, and then select the waveform analysis tools to analyze the waveforms.

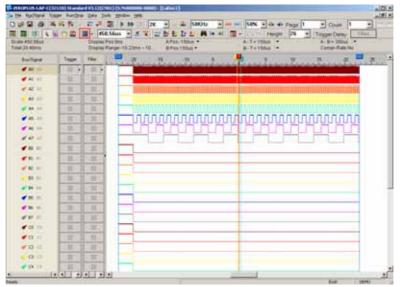


Fig 4-25 – Click 📓 Icon to View All the Data

3. Stop to end Run

Click the Stop <a>[icon to end the Run.

Tip: If the status is "Waiting..." with no signal outputting as shown in Fig 4-26, click the Stop icon to end the Run; check the setup again, and try the run process again.

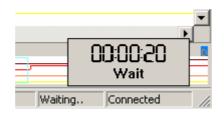


Fig 4-26 - Waiting Status



4.2 Bus Logic Analysis

Section 4.2 presents detailed instructions about logic analysis with a set of grouped signals, which is known as Bus Logic Analysis.

Basic Software Setup of the Bus Logic Analysis

- Step1. Set up the RAM Size, Frequency, Trigger Level and Trigger Position as described in Section 4.1.
- Step2. Group signals into a Bus

Click **Channels Setup** on Bus/Signal of the menu bar, or click icon. The dialog box shown in Fig 4-27 will appear.

Signal Fill				T	A	N Du	154	NR.	1						1		Dele	le A	i.	1		nić;	in De	(nA	R)					
Group int	Fish	T	-		Part 1	0	-	-			-	at	0	-	-				P	1	-			T			-	À.		
Ungroup	To Condition	100		ł					-				10	8			5				ä	-							í	
131-2-11	Bus1	7	5	5	4	7		9	3	-6	5	4	3	2	1	0	7	6	5	4	킍	2	1 0	12	5	5	1	3	2	
Expand	A2 A3 A4 A5 A5 A5 B0	7	2	2	2	41		0	H	ię,	뎒	4	4	ŝ	÷	0	1	1		÷	ŝ.	51	1.1	K	iê.	12	1	÷.	5	11
Collapse.	A4	7	8	5	4	31.	15	6	12	14	5	4	-3	2	1	0	7	8	5	4	3	211	1 0	7	8	5	18	3	2	1 (
CONSIST	A5	7	4	5	4	1.		. 0	12	1	1	4	1	2	1	Ű	7	5	5	4	1	20	1.1	2	1	7	-	3	2	1 1
Format R	A6	14	2	2	4	섞음	1	10	14	12	2	1		4	4	.0	+	승님	옷	2	4	÷.,	113	14	17	2	-	-	1	
PORMAC R	Bil	12	÷	5	1	11		1 a	铃	12	18	4	3	2	÷.	0	7	1	\$	4	51	21		17	12	1X	4	5	2	1 1
Rename	Coat	1	1	*	1	1.1	100	1	1	1		1	1	1.	1	1	11	1	1	1	1	105	1.1		1	1	1	2		1 1

Fig 4-27 – Channels Setup

Rename the Bus and set up the channels of the Bus as shown in Fig 4-28.

Port				Po	rt E			F	Port /	Α			
Tr.Condition	8	\mathbb{X}	\sim	\sim	1		\mathbb{X}	\mathbb{X}		\mathbb{X}	\mathbb{X}	\mathbb{X}	
Fi.Condition		\mathbb{X}		\mathbb{X}	12							\mathbb{X}	X
Bus1	7	6	5	4	З	7	6	5	4	3	2	1	0
A2	7	6	5	4	З	7	6	5	4	3	2	1	0
A3	7	6	5	4	З	7	6	5	4	3	2	1	0
A4	7	6	5	4	З	7	6	5	4	3	2	1	0
Bus2	7	6	5	4	З	7	6	5	4	3	2	1	0
A6	7	6	5	4	З	7	6	5	4	3	2	1	0
A7	7	6	5	4	З	7	6	5	4	3	2	1	0
B0	7	6	5	4	3	7	6	5	4	3	2	1	0
Assignment Count	1	1	1	1	1	1	1	1	1	1	1	1	1

Fig 4-28 – Rename Bus

1. Click the column, then type the given name of the Bus, and then press Enter to confirm it.

2. Go to the relative channels as shown in the example and go to numbers 0, 1, 2, 3, which are located on column A and row Bus1. Click them to become purple, then set these segments of channels.

3. Click **OK** to get the result as shown in area 1.

	AO AO				(L	Add	Bus,	Sign	val .	2	D8	etel	GU SŢI	in.	1		De	lete /	4	-	Re	estor	e Del	lauk	\$	>				
-0	100000 (1440)	Ξ,	Port			P	ort E	9				- 2	F	Port C						P	ort 8						P	A ho	-		5
.0	A2 A2	- <	Freenation	122	201	× 2	9.0	9 83	28	124	X	10	00	4	×.	8	<u>19 0</u>	9 P.	29	23	29	<u>X 9</u>	9 (X	2. (X	25	22	82	257 1	SER.	1.00	>
e	Bus1 A3	<	Pecondition	1.01	04		N K	5	19		la.	101	101	iai				1.5		ici.	64			0	10	10	NO.	KOA N	SI, K	1.00	5
V	A4 1	1	A0 A2	7	6	54		3 2	1	0	777	6	5 5	4	3 3	2 2	1 (6	5 5 5	4	3	2 1	0	7	6	5 5	4	3 2	1	0
	. A0	AO	But	7	6	54		3 2	1	7	777	6	5	4	3	2 2	1 (6	5 5	4	3 3	2 1	0	777	6	5	4		1	0
	🗢 A1	A1	A5 A6	777	6	5 4		3 2	1	0	77	6	5 5	4	3	2	1 (-	6	5	4	3 3	2 1	0	7	6	5	4	3 2	1	0
	e A2	42	A7	7	6	5 4	1.3	3 2	1	0	7	6	5	4	3	2	1 (7 0	6	5	4	3 3	2 1	0	Z	6	5	4	3 2	1	0
	C A3	A3	Count										1			1020				100				100		10	-			11	-
	C A4	A4	Reserve		383	10.000	322	2007	1717	8																					

Fig 4-29 – Channels Setup Window

Tip: Channels Setup

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Zeroplus Technology Co., Ltd.

In the dialog box of Channels Setup, there isn't only Add Bus/Signal, but also Delete Bus/Signal, Delete All, Restore Defaults provided.

- 1. Delete Bus/Signal: Firstly highlight the Bus or channels on area 6 of Fig 4-29, then click **Delete Bus/Signal** to delete them.
- 2. Delete All; Click Delete All to delete all Bus/signals on area 6 of Fig 4-29.
- 3. Restore Defaults: Click **Restore Defaults** to restore the dialog box of Channels Setup as shown in Fig 4-27.

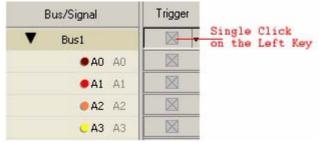
Step3. Trigger Condition Setup

1. Highlight the Bus which will be triggered then click 📌 icon or select **Bus Trigger Setup** from the Trigger of the Menu Bar, the dialog box as shown in Fig 4-30 will appear.

Bus	Trigger			×
В	us Trigger Protocol A	nalyzer Trigger		
ſ				
	Bus Name	Operator	Value	
	Bus1 👻	=	▼ 1E	_
	Data Farmat			
	Data Format		C D : KO: D	
	C Binary	🔿 Decimal	O Decimal(Signed)	
	Hexadecimal	C ASCII	🔘 Gray Code	
	C Complement			
Ľ				
	OK	Cano	el Default	Help

Fig 4-30 - Bus Trigger Setup

Tip: Left click on Trigger column of the Bus as shown in Fig 4-31.



- Fig 4-31 Trigger Column
- 2. Set Binary, Hexadecimal, Decimal, Decimal(signed), ASCII, Gray Code or Complement as the Data Format of the Bus to represent the value (see Fig 4-30).
- 3. Set "=" and "Don't Care", and type the value of the Bus into Value column to set the trigger condition



of the Bus.

4. Click **OK** to confirm the settings.

- **Step4.** Click **Run** and activate the signal from the tested board to the system to get the result as shown in Fig 4-32.
 - Tip: Click 📓 icon to view all data, and then select the waveform analysis tools to analyze the waveforms.

Set **Value** is "2" as Hexadecimal, and set **Operator** equals to "=", then click **OK**. Click **Run** and activate the signal from the tested board to the system to get the result as the trigger happens on 0X2.

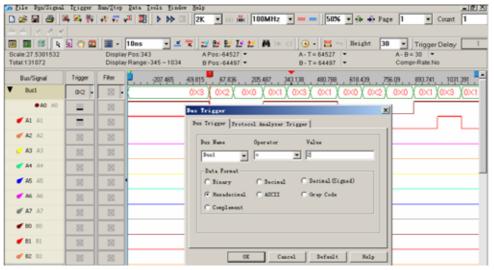


Fig 4-32 – Bus Trigger Setup

4.3 Plug Analysis

Plug Introduction

Protocol Analyzer operates in the form of Plug; every Protocol Analyzer has a plug, per plug is independence modularization. One Protocol Analyzer plug can analyze many Buses at the same time, however, because the independence of every plug, the Protocol Analyzer plug only supports I2C, UART, SPI, HDQ, 1-WIRE, CAN 2.0B at present. In the future, it will support more Buses, and when the Protocol Analyzer renews, it only needs to download the new Protocol Analyzer plug to cover the old Protocol Analyzer plug; the speed is very fast.

Operating Instructions: There are PlugIns data file in the position of installing LA software. All Protocol Analyzer plugs which are used at present are put in the data file, the DLL file can be added or deleted in the content, and in the Bus property, all Protocol Analyzer plugs that can be used at present can be seen as the figure below:

PluginsA			_		the second s	
Ain feit Very Poverts	is tests the					10
4- teck - + - 31 Q	Seath Bridges Beatory	進船 X 約1	28·			1 - C
Address 🗋 Pluy, Dis A						- 1960. -
	PhopierRE, cl. PhopCARELS	809003 A	B anca	Pugs?Lal	छ भ्यू-भारत	2211
Select an ten to view its description.	-0					
Hir Conservation Hir Conservation Hir Computer						

Fig4-33 - PlugInsA

🖱 Bus		Color Config	J
Activate the Latch Function		AO	
		Rising Edge	
rotocol Analyzer Setting			
Protocol Analyzer ZEROPLUS LA 1-WIRE MODULE ZEROPLUS LA 3-WIRE MODULE ZEROPLUS LA A-GOZ MODULE VI	V1.04.00(CN01)	Parameters Co	nfig
C ZEROPLUS LA 1-WIRE MODULE	V1.04.00(CN01) .02.00(CN01) DGIC MODULE V1.51. 00.00(CN01) E V1.32.00(CN01) E V1.31.00(CN01) I MODULE V1.01.00(DULE V1.00.00(CN01)	00(CN01) CN01)	nfig

Fig4-34 - Bus Property

Every Logic Analyzer Module can provide some basic Protocol Analyzer plugs. When users need to use the analysis which is not provided by the basic Protocol Analyzer plugs, you can purchase from our company, and then, you can get this Protocol Analyzer plug and the register code.



STEP 1. Put the CAN 2.0B Plug in the PlugIns as the Fig4-35.

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eth 凸fides (Jhatey) 復 弘 X 21 (田•	
	न लेक
છે. છે. છે. છે. છે. છે. ગંદ્રાઓકદલ મહ્લ્યાસ્થા મહ્લ્યાસ	
-	
	PlugtWIRE of FlugCANBUS PlugHDQ of PlugDC.of PlugSPC of PlugUART.of

Fig4-35 - PlugInsA

STEP 2. Select CAN 2.0B in the Protocol Analyzer list.

Bus Setting	
C Bus	Color Config
Activate the Latch Function	Rising Edge
Protocol Analyzer Setting	
Protocol Analyzer	Parameters Config
ZEROPLUS LA CAN 2.08 MOD	OULE V1.32.00(CN01)
C ZEROPLUS LA 12C(EEPROM 2	24LC561/24LC562) MODULE V1.00.00(CN01)
C ZEROPLUS LA I2C MODULE V	/2.01.03
C ZEROPLUS LA LG4572 MODU	LE Y1.00.00(CN03)
C ZEROPLUS LA PECE MODULE	V1.11.00(CN01)
C ZEROPLUS LA PT2262/PT227	2 MODULE V1.00.00(CN01)
C 750 COLLIS LA \$20mm/052C	wire MODULE V1.00.00(CN01)
LO SERONDOS DA SECALICIASEC	1 11 02
C ZEROPLUS LA SPI MODULE Y	1.11.00
C ZEROPLUS LA SPI MODULE Y	E V2.13.00(CN01)



STEP 3.Click Parameters Configuration button, select Register and enter the Serial Key.

PROTOCOL ANALYZER CAN 2.08		×
Configuration Packet Data Format	Register	
The CAN 2.08 protocol analyzer dec	oding function is an optional purchased say to activate this function for your necessary.	
	tions about ordering software please follow the les team will respond to your enquity as soon as 886-2-66202225	
>> Applications through Email	service_2@zeroplus.com.tw	
>> Website:	http://www.zeroplus.com.tw	
Copyright(C) 1997-2012 ZEROPLUS	TECHNOLOGY CO.,LTD.	
	OK. Cancel Default H	lelp

Fig4-37 - Protocol Analyzer CAN 2.0B Register dialog box



4.4 Bus Packet List

Bus Packet List is a graphics list which is used for doing Statistics and showing Bus Packet List. It is visual and direct, especially for I2C, USB 1.1 and CAN 2.0B. When there is a packet list, it gets twice the result with half the effort to check the data. Packet List has its startup button in Toolbar. After starting it, it will show a small window under the waveform window. Users can alter its size to find more data.

Notice: If you want to learn more about the Bus Packet List, please refer to the Specification of the Protocol Analyzer.

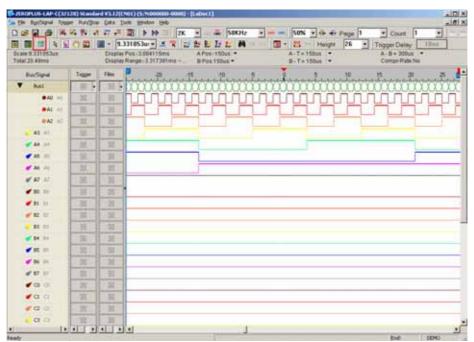


Fig	4-38	-	Packet	Icon

Harf Spraf Display Foc- 2044 (Smith A - Bit - 200x1 * A - Bit - 200x1 * Bit 23 - 40m Display Foc- 2044 (Smith B + T = 150x1 * A - Bit - 200x1 * Bit 23 - 40m Display Foc- 2044 (Smith B + T = 150x1 * B - T = 150x1 * Bit 25 - 40m B + T = 150x1 * B + T = 150x1 * Corrup Faith for Bit 25 - 40m B + T = 150x1 * Display Foc- 2044 (Smith Display Foc- 2045 (Smith Bit 25 - 40m B + T = 150x1 * Display Foc- 2045 (Smith Display Foc- 2045 (Smith Display Foc- 2045 (Smith A + A = -40m B + -40m B + -40m B + -40m Display Foc- 2045 (Smith		0.00	-	131053		1		L L	M	()]]		100 C	Hoight	26 •	Trigger Delay	
Note Image: Control of the																
40 5 5 7 0 1 2000 44 4 5 6 7 0 1 2000 44 4 5 6 7 0 1 2000 45 6 7 0 1 200 1000	MATERIA .	Trigger	Film		-20		15	(E10)		e)	F.		1	30	.8	()
•44 •	Rat	1	1.25	000	300	100	XXX	XXX	XXX	000	000	202	000	XXXX	XXXXX	0000
#42 #	•A0 ==	20	-12	пп			ПГ	П	ПГ		пп	ПГ	101			100
43 41 10 10 44 41 10 10 44 41 10 10 45 41 10 10 45 41 10 10 45 41 10 10 45 41 10 10 46 41 10 47 41 10 48 10 49 41 40 41 41 10 41 10 42 10 43 10 44 44 45 45 46 46 47 10 48 10 49 47 49 48 49 48 40 48 40 48 41 48 41 42 48 43 48 44 48 45 48 46 48 47 48 48 48 49 48 49 48 48 49 <	BAL AL	5.88.5	1.28			1										
An AI Bit Bit Bit Bit Bit	#A2 40	22	- 25			-		F								
A m M	AS #1		35	1												10.000
A A B B 4 A A A A 4 A A A A A 4 D A A A A 4 D A A A A 4 D A A A A 4 D A A A A 4 D A A A A 4 D A A A A 4 D A A S A S A 4 D A B A S A S A A 4 D A S A S A <td># AA</td> <td>22</td> <td>30</td> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>1</td> <td></td> <td></td> <td></td> <td>1</td>	# AA	22	30	-								1				1
4 47 A1 10 11	# A5 10	1.66	25	-												-
 ▲ 0 ▲ 0	# M 20	32	32													
Money Money <th< td=""><td># 47 13</td><td>- 58</td><td>1.21</td><td></td><td></td><td></td><td>-</td><td>_</td><td></td><td></td><td>_</td><td></td><td></td><td></td><td></td><td></td></th<>	# 47 13	- 58	1.21				-	_			_					
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Bit of State State <t< td=""><td># N2 11</td><td>100</td><td>58</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></t<>	# N2 11	100	58													
Infrard Control Data		- 10		-												
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2 Buildua) -10.13ma 2 3 4 5 6 7 0 1 2 3 100.m	ettru Refresh	Equit		Let a	The second			4	5	6	7	- G	1			
	ettra Rafredi	Equit.	129ms	C-sta 0	Duts 1	2	3				Contraction of the	CONTRACT	T1070	THE R. LEWIS CO., LANSING MICH.		
	eting Refresh Pachet # Nor 1 (bus10) Packet # Nor	Expert-	netilanp 129ms Helitanp	Cata	Deta	Date	Date	Date.	-	Cliffe		_				
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Fig4-39 - Bus Packet List

Packet List has a setup window; users can set up the Packet List according to their requirements. Setting Bus Packet Length in dialog box is only used for doing Bus Statistic. Users can define how long the time is as a



data packet to add the export function. See the following figure.

Setting			×
-Bus Select	Data Format		
✓Bus1(Bus)	C Binary	O Decimal	
	\bigcirc Decimal(Signed)	• Hexadecimal	
	C ASCII	🔘 Gray Code	
	C Complement		
	-Bus Packet Length		
	100mm	in: 10ms ax: 20.48s	
Packet Item			
Packet IV Name	Z TimeStamp Len	oth Data	
	- ninescamp - con		
Text			
• • • • • • • • • • • • • • • • • • •	t Color Auto		
ОК	Cancel Defaul	t Help	

Fig4-40 - Packet List Setting

Setting	Refresh Expo	rt Synch Pa	rameter										
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length
1	Bus1(Bus)	-10.23s	0	1	2	3	4	5	6	7	0	1	100ms
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length
2	Bus1(Bus)	-10.13s	2	3	4	5	6	7	0	1	2	3	100ms
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length
3	Bus1(Bus)	-10.03s	4	5	6	7	0	1	2	3	4	5	100ms
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length
4	Bus1(Bus)	-9.93s	6	7	0	1	2	3	4	5	6	7	100ms
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length



1. View Specifications

Packet #, Name and TimeStamp can be selected to display from the Packet List Setting dialog box.

Packet #: List the order of Packet.

Name: Display the name of Packet, or the Filter Display Bar.

TimeStamp: It is the starting point of the Packet.

Tip: The rest name and content are supplied by Plug.



× ∥	Setting	Refresh Expo	rt Synch Pa	rameter													
	Packet #	Name	TimeStamp	ADDRESS	Write	A-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	
	1	Bus1(I2C)	-1us	50	Write	A-ACK	00	D-ACK	75	D-ACK	01	D-ACK	23	D-ACK	45	D-ACK	
	DA	TA D-ACK															
	6	7 D-ACK															
	Packet #	Name	TimeStamp	ADDRESS	Write	A-ACK	DATA	D-ACK	DATA	D-ACK							
	2	Bus1(I2C)	10.2064ms	50	Write	A-ACK	00	D-ACK	75	D-ACK							
	Packet #	Name	TimeStamp	ADDRESS	Read	A-ACK	DATA	D-NACK	DESC	RIBE							
	3	Bus1(I2C)	10.2982ms	50	Read	A-ACK	01	D-NACK	DATA	NACK							
	Packet #	Name	TimeStamp	ADDRESS	Read	A-ACK	DATA				DATA	D-NACK	DESC				
	4	Bus1(I2C)	10.3554ms	50	Read	A-ACK	23	D-ACK	45	D-ACK	67	D-NACK	DATAN	IACK			
	Packet #	Name	TimeStamp	ADDRESS	Write	A-ACK	DATA		DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	
	5	Bus1(I2C)	20.477ms	50	Write	A-ACK	00	D-ACK	79	D-ACK	89	D-ACK	AB	D-ACK	CD	D-ACK	J
	DA																
	E	F D-ACK	l														
																	•

Fig4-42 - Protocol Analyzer I2C Packet List

Setting: It is used to open Packet List Setting dialog box.

Refresh: Press this button, the list view can renew automatically.

Export: Export the workspace into Text (*.txt) and CSV Files (*.csv).

Synch Parameter: Open the synch parameter setting dialog box and activate the packet and waveform synch function.

2. Display Protocol Analyzer Packet in Order

Tip: The below view are Protocol Analyzer I2C; the packet is determined by the position of the TimeStamp.

× ∥	Setting	Refresh Exp	ort Synch Pa	ameter													
	Packet #	Name	TimeStamp	ADDRESS	Write	A-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	
	1	Bus1(I2C)	-1us	50	Write	A-ACK	00	D-ACK	75	D-ACK	01	D-ACK	23	D-ACK	45	D-ACK	
	DA 6	TA D-ACK								-	_						
	Packet #	Name	TimeStamp	ADDRESS	Write	A-ACK	DATA	D-ACK	DATA	D-ACK							
	2	Bus1(I2C)	10.2064ms	50	Write	A-ACK	00	D-ACK	75	D-ACK	J						
	Packet #	Name	TimeStamp	ADDRESS	Read	A-ACK	DATA	D-NACK	DESC	RIBE							
	3	Bus1(I2C)	10.2982ms	50	Read	A-ACK	01	D-NACK	DATAN	JACK							
	Packet #	Name	TimeStamp	ADDRESS	Read	A-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-NACK	DESC	RIBE			
	4	Bus1(I2C)	10.3554ms	50	Read	A-ACK	23	D-ACK	45	D-ACK	67	D-NACK	DATA N	IACK			
	Packet #	Name	TimeStamp	4.DDRESS	Write	A-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	DATA	D-ACK	
	5	Bus1(I2C)	20.477ms	50	Write	A-ACK	00	D-ACK	79	D-ACK	89	D-ACK	AB	D-ACK	CD	D-ACK	
	DA	TA D-ACK															
	E	F D-ACK															
		•	-														
																	-



Tip: When the Display Bar of Signal Filter is activated, the Bar should be displayed in the Bus Packet List, and also the TimeStamp, ADDRESS and length of the Bar will be displayed.

3. Packet Idle and Packet Length

Packet Idle: Packet interval time Packet Length: Packet time length

When those above two items are to be displayed, it only chooses one of them to display, which is controlled by Plug.

Because it is impossible that every Protocol Analyzer packet has registered timestamp and end, we add two special Unknow_Flag to judge the timestamp and end of the packet which are Unknow _Start_Flag and Unknow_End_Flag.



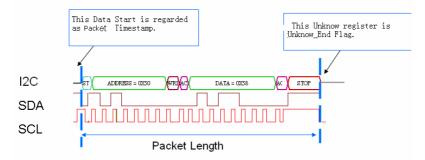


Fig4-44 - Protocol Analyzer I2C Packet Length

Tip: Because I2C has started as the Packet TimeStamp, it does not need to use Unknow_Start_Flag as the start.

4. Bus

Setting	Refresh Expo	Synch Pa	rameter											
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
1	Bus1(Bus)	-10.23s	0	1	2	3	4	5	6	7	0	1	100ms	
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
2	Bus1(Bus)	-10.13s	2	3	4	5	6	7	0	1	2	3	100ms	
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
3	Bus1(Bus)	-10.03s	4	5	6	7	0	1	2	3	4	5	100ms	
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
4	Bus1(Bus)	-9.93s	6	7	0	1	2	3	4	5	6	7	100ms	
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
5	Bus1(Bus)	-9.83s	0	1	2	3	4	5	6	7	0	1	100ms	
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
6	Bus1(Bus)	-9.73s	2	3	4	5	6	7	0	1	2	3	100ms	
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
7	Bus1(Bus)	-9.63s	4	5	6	7	0	1	2	3	4	5	100ms	
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	

Fig4-45 - Bus Packet List

Packet Length and Packet Idle Length

Packet's TimeStamp is the start of Bus Data; the default length is controlled by the setting dialog box. If the input packet length isn't the end of data. The software will prolong the length of Packet to end the data automatically as the figure below.

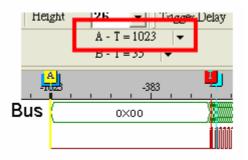


Fig4-46 - Auto-Prolong Packet

The Fig4-46 is a Bus; its first data is 0x00, and its length is 1023. If users input 20 as the Bus length. But 20xaddress is not the end of this data, so the software will prolong the length of the Packet to 1023 automatically.





Fig4-47 - Packet End

The Fig4-47 is a Bus. If the Start of the packet is T bar and the set Bus length is 20, but the data 0x02 isn't the end, at that time, the Packet will be prolonged to the end dot automatically, that is to say, the Address 27 (B bar) is the End of the packet.

The above two data are made consecutively as the figure below.

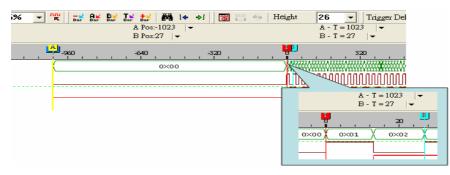


Fig4-48 - Auto-Prolong Packet

The Packet List is displayed as the figure below:

Setting	Refresh Expo	ort Synch Pa	rameter										
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length
1	Bus1(Bus)	-10.23s	0	1	2	3	4	5	6	7	0	1	100ms
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length
2	Bus1(Bus)	-10.13s	2	3	4	5	6	7	0	1	2	3	100ms
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length
З	Bus1(Bus)	-10.03s	4	5	6	7	0	1	2	3	4	5	100ms
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length
4	Bus1(Bus)	-9.93s	6	7	0	1	2	3	4	5	6	7	100ms
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length
5	Bus1(Bus)	-9.83s	0	1	2	3	4	5	6	7	0	1	100ms
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length
6	Bus1(Bus)	-9.73s	2	3	4	5	6	7	0	1	2	3	100ms

Fig4-49 - Bus Packet List

Tip: The Protocol Analyzer Packet will be explained in the following plug.

5. Packet and Waveform Synchronization

For the convenience of fast corresponding between packet data and waveform data, and what is more, in order to make it easier for users to look up data, we add the Packet and Waveform Synchronization function.

In order to operate conveniently, we add a Synch Parameter button on the BUS Packet List as the image below:

Setting	Refresh Expo	ort Synch Pa	rameter											
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
1	Bus1(Bus)	-10.23s	0	1	2	3	4	5	6	7	0	1	100ms	
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
2	Bus1(Bus)	-10.13s	2	3	4	5	6	7	0	1	2	3	100ms	
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
3	Bus1(Bus)	-10.03s	4	5	6	7	0	1	2	3	4	5	100ms	
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
4	Bus1(Bus)	-9.93s	6	7	0	1	2	3	4	5	6	7	100ms	
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
5	Bus1(Bus)	-9.83s	0	1	2	3	4	5	6	7	0	1	100ms	
Packet #	Name	TimeStamp	Data	Data	Data	Data	Data	Data	Data	Data	Data	Data	Length	
6	Bus1(Bus)	-9.73s	2	3	4	5	6	7	0	1	2	3	100ms	

Fig 4-50 - Synch Parameter on the BUS Packet List

At the same time, a Synch Parameter Setting dialog box is added.

Synch Parameter Setting	×
Activate Packet and Waveform	Synch
Synch Point of Packet List	Synch Point of Waveform Area
• Тор	C Left
C Middle	 Middle
	OK Cancel

Fig 4-51- Synch Parameter Setting Dialog Box

Activate Packet and Waveform Synch: The default is not activated.

Top: When the Packet and Waveform Synch is activated, the synch point in Packet List is the top packet segment which is displayed by list.

Middle: When the Packet and Waveform Synch is activated, the synch point in Packet List is the middle packet segment which is displayed by list.

Left: When the Packet and Waveform Synch is activated, the synch point in the waveform area is the left packet segment which is displayed by waveform.

Middle: When the Packet and Waveform Synch is activated, the synch point in the waveform area is the middle packet segment which is displayed by waveform.

Activate Packet and Waveform Synch, select Top and Left.

Synch Parameter Setting	×
Activate Packet and Waveform	Synch
Synch Point of Packet List	Synch Point of Waveform Area
• Тор	© Left
O Middle	C Middle
	OK Cancel

Fig 4-52 - Synch Parameter Setting Dialog Box



Display the corresponding waveform and packet as below image:

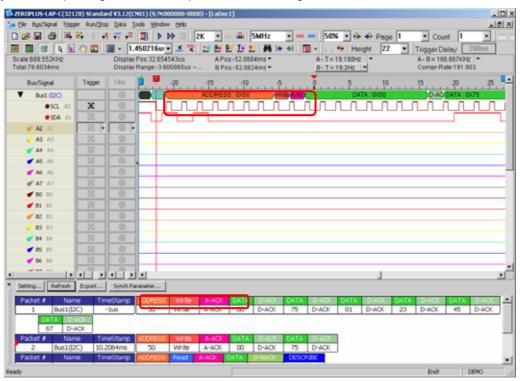


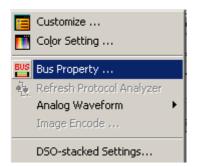
Fig 4-53 - Waveform and Packet Synchronization Interface



4.5 Bus Analysis

The setup is correlated to the Bus which needs to be made up, for example: Bus, Protocol Analyzer. Open the dialog box:

STEP 1.Click **Tools** on the Menu Bar, and then select **Bus Property** or select **bus** to set up Bus Property.



50%	🔽 🎋 📣 Page	1
BUS a	Height 22	-

Fig4-54 - Bus Property on Menu Bar

Fig4-55 - Bus Property on Tool Bar

STEP 2.Click the **Right Key** on the Bus/Signal column, and then select **Bus Property**.

Tip: The signals must be grouped into Bus, or the Bus Property can not have effect.

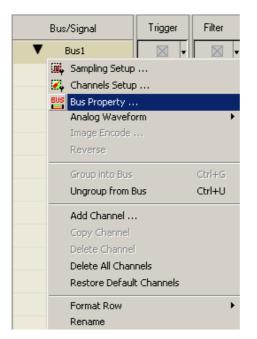


Fig4-56 - Right Key to Set Bus Property



4.5.1 Bus Analysis

The Bus Analysis function enables the system to analyze the Bus.

Basic Software Setup for the Bus

STEP 1. Click **Bus Property**, the following dialog box will appear.

is Property	
Bus Setting Bus Activate the Latch Function	Color Config
Protocol Analyzer Setting	,
C Protocol Analyzer	Parameters Config
 ZEROPLUS LA 1-WIRE MODULE V1.10.00(CN01) ZEROPLUS LA 3-WIRE MODULE V1.04.00(CN01) ZEROPLUS LA AC97 MODULE V1.02.00(CN01) ZEROPLUS LA ARITHMETICAL LOGIC MODULE V1.51. ZEROPLUS LA BUS MODULE V1.00.00(CN01) ZEROPLUS LA CAN 2.0B MODULE V1.32.00(CN01) ZEROPLUS LA CCIR656 MODULE V1.31.00(CN01) ZEROPLUS LA COMpact Flash 4.1 MODULE V1.01.00(0) ZEROPLUS LA CMOS IMAGE MODULE V1.00.00(CN01) 	CN01)
🔽 Use the DsDp	Find
More Protocol Analyzer	Cancel Help

Fig4-57 - Bus Setting

STEP 2. Click Color Configuration to set **Bus Data Color**.

Bus	Color Config
Activate the Latch Function	AO
	Rising Edge 💌
Protocol Analyzer Setting	
O Protocol Analyzer	Parameters Config
C ZEROPLUS LA 1-WIRE MODULE V1.10.00(
C ZEROPLUS LA 3-WIRE MODULE V1.04.00(· · · · · · · · · · · · · · · · · · ·
CZEROPLUS LA AC97 MODULE V1.02.00(CN	· · · · · · · · · · · · · · · · · · ·
ZEROPLUS LA ARITHMETICAL LOGIC MOD C ZEROPLUS LA BUS MODULE V1.00.00(CN0)	
ZEROPLUS LA CAN 2.08 MODULE V1.32.00	· ·
CZEROPLUS LA CCIR656 MODULE V1.31.00	
C ZEROPLUS LA Compact Flash 4.1 MODULE	V1.01.00(CN01)
C ZEROPLUS LA CMOS IMAGE MODULE V1.0	· · · · · · · · · · · · · · · · · · ·
	Find
🔽 Use the DsDp	

Fig4-58 - Color Configuration



Bus Data Color	×
Bus Name: Bus1	
Data Condition: Data Min:	Data Max:
= 0	7
Select Color:	
Cancel	Default Help

Fig4-59 - Bus Data Color

Bus Name: Display the selected Bus name.

Data Condition: Select the Data Condition to change the Bus data color. There are four options which are = , !=, In Range and Not In Range.

Data Min: Enter the min. data that is required by users.

Data Max: Enter the max. data that is required by users. The max. data can be used only when the set is In Range or Not In Range.

Select Color: Select the changed color according to the Bus condition set by users, the default is Green.

STEP 3. Click **Color Configuration** to open the Bus Data Color dialog box, and set the "Data Condition = 0" and Select Color is Orange.

Bus Data Color	×
Bus Name: Bus1	
Data Condition: Data Min:	Data Max:
= 0	F
Select Color:	
OK Cancel	Default Help

Fig4-60 - Set the Color for Bus1

Bus/Signal	Trigger	Filter	₽ -20) -15	-10	-5	·
▼ Bus1	•	•	(<u>0x1</u>)	0X2 X 0X3) 0X4	0X5 (0X6	(0X7)
• A0 A0							
●A1 A1							

Fig4-61 - Before the Bus Data Color Setting

Bus/Signal	Trigger	Filter	-20 -15 -10 -5 0 5	10
▼ Bus1	•	•		0X0
• A0 A0				
• A1 A1				

Fig4-62- After the Bus Data Color Setting

Tip: Reserve the original state by the above steps.

STEP4. Activate the Latch Function



Activate the Latch Function: The default is not activated. When the Latch function is activated, the default channel is A0, and there are three conditions for selecting, Rising Edge, Falling Edge and Either Edge; the default is Rising Edge.

Tip: The Latch function is available for the LAP-321000U-A, LAP-322000U-A, LAP-C(162000), LAP-C(321000) and LAP-C(322000)Modules, and it is not available for the LAP-16032U, LAP-16064U, LAP-16128U, LAP-32128U-A, LAP-C(16032), LAP-C(16064), LAP-C(16128) and LAP-C(32128) Modules.

Set the Latch function for one Bus. The setting of the Latch channel is A0; the analysis function adopts Rising Edge.

	Color Config					
Activate the Latch Function	A0 💌					
	Rising Edge					
Protocol Analyzer Setting						
O Protocol Analyzer	Parameters Config					
C ZEROPLUS LA 1-WIRE MODULE V1.1						
ZEROPLUS LA 3-WIRE MODULE V1.0 CEROPLUS LA AC97 MODULE V1.02.0						
C ZEROPLUS LA ARITHMETICAL LOGIC						
C ZEROPLUS LA BUS MODULE V1.00.00						
C ZEROPLUS LA CAN 2.08 MODULE V1.						
C ZEROPLUS LA CCIR656 MODULE V1.31.00(CN01)						
ZEROPLUS LA Compact Flash 4.1 MO C ZEROPLUS LA CMOS IMAGE MODULE						
C SERVITED EN CHOS THINGE HODOLE	· · · · · · · · · · · · · · · · · · ·					
# 200 ODUICEA DALT T-K-S MODU						

Fig4-63 - Activate the Latch Function

The picture of the waveform analysis:

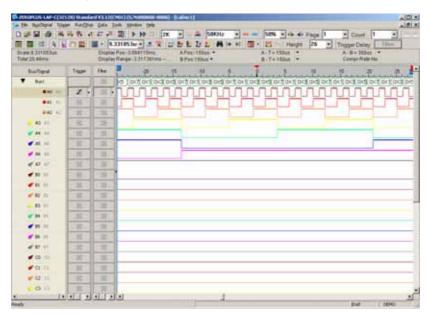


Fig4-64 - The Latch Function Displayed on the Waveform Area

Illustration: The selected channel is A0; the analysis mode is Rising Edge; it indicates that the data of the A0 is read at the Rising Edge. See the T Bar in the above figure, the data of Bus1 is 0X3.

4.5.2 I2C Analysis

I2C Introduction

The I2C, which stands for Inter-Integrated Circuits, is a serial synchronous half-duplex communication protocol. The I2C was first proposed by Philips Semiconductor Netherlands. This I2C protocol consists of a very simple physical interface which has only two signal channels, SDA (Serial Data) and SCL (Serial Clock). Most I2C devices consist of an independently sealed I2C chip, and this I2C chip has direct connection to both SDA and SCL. The data transmission is a byte-base (8-bit base) for every segment. Since many oscilloscopes do not allow engineers to observe timing sequence information directly from the screens of oscilloscopes, this Logic Analyzer was created to help engineers resolve timing sequence issues during their circuit development.

I2C has a multi-control Bus as its physical and firmware interfaces. This protocol analyzer is basically a signal network that may connect to one or several control units. The intention of inventing this protocol was in the application of designing television sets, which allowed the central processing unit to quicken data communications with peripheral chips and devices. The I2C interface is initiated with a SDA triggered **High** and SCL triggered **Falling Edge**. Following the initiation, there will be a set of 7 bits (or 10 bits) address space. Beyond this point, there will be Read/Write, ACK (Acknowledgement), and STOP (or HALT/HLT). The signal information packet is transmitted in bytes. If there are two or more devices trying to access the I2C protocol, whichever device has SCL at logic high will gain access priority.

Furthermore, since I2C is a synchronous communication protocol and data transmission must be in bytes, a complete I2C signal packet must consist of **Start**, **Address**, **Read/Write**, **Data**, **ACK/NACK** and **Stop** segments. They are as following.

Start: This is the initiation of SCL and SDA (1 bit only).
Address: This identifies the device address (7 bits).
Read/Write: This is a data direction bit. 0 = Write, 1 = Read.
ACK/NACK: This is a confirmation bit following every data transmission segment.
Data: The actual signal data transmitted by byte.
Stop: This appears when SCL = High and SDA = Low (1bit only).



4.5.2.1 Software Basic Setup of Protocol Analyzer I2C

Step1. Set up RAM Size, Frequency, Trigger Level and Trigger Position as described in Section 4.1.

- **Step2.** Set up the Falling Edge as the trigger condition on the signal which connects to the tested I2C data pin (SDA).
- Step3. Group the analytic channels into Bus1.

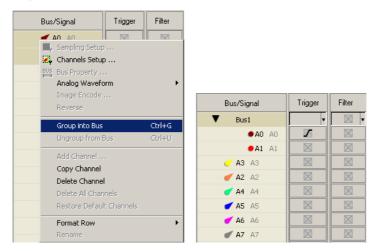


Fig4-65 - Group into Bus

Step4. Select Bus 1, then, press **Right Key** on the mouse to list the menu. Next, click **Bus Property** or click **Tools** and the select Bus Property or click ^{Bus} to open Bus Property dialog box.

	Bus Property	×
	Bus Setting	
	 Bus 	Color Config
Bus/Signal Trigger Filter	Activate the Latch Function	A0 🗸
Busi 🔍 🗸 🕅		Rising Edge
Sampling Setup	Protocol Analyzer Setting	
Channels Setup Bus Property	O Protocol Analyzer	Parameters Config
Analog Waveform Image Encode Reverse	CZEROPLUS LA 1-WIRE MODULE V1.10.00(CN01) ZEROPLUS LA 3-WIRE MODULE V1.04.00(CN01) ZEROPLUS LA AC97 MODULE V1.02.00(CN01)	
Group into Bus Ctrl+G Ungroup from Bus Ctrl+U	ZEROPLUS LA ARITHMETICAL LOGIC MODULE VI ZEROPLUS LA BUS MODULE V1.00.00(CN01) ZEROPLUS LA CAN 2.08 MODULE V1.32.00(CN01))
Add Channel Copy Channel Delete Channel	ZEROPLUS LA CCIR656 MODULE V1.31.00(CN01) ZEROPLUS LA Compact Flash 4.1 MODULE V1.01. ZEROPLUS LA CMOS IMAGE MODULE V1.00.00(C) ZEROPLUS LA CMOS IMAGE MODULE V1.00.00(C)	00(CN01) N01)
Delete All Channels	Use the DsDp	Find
Restore Default Channels	More Protocol Analyzer	
Format Row Rename	C OK	Cancel Help

Fig4-66 - Bus Property

Step5. For Protocol Analyzer Setting, select Protocol Analyzer. Then, choose **ZEROPLUS LA I2C MODULE V2.02.00 (CN01)**. Next, click **Parameters Configuration**. The following image will appear.



Configuration Timing Packet Data Format Register											
Pin Assignment		Data Mode	,								
-	-	Item	N	lame D	ata Length						
SDA: A0	Slave	Addr: Ad	śdress 🛛	7	bit .						
SCL: A1	*	E Re	g Addr: Re	g Addr	8	ЬR —					
		Data:		Data	8	ы					
Protocol Analyzer Prop	erty										
Write Bit 💌	Low Level	E Do	n't stop analyzin;	g when NACK	appears						
ACK 💌	Low Level	Add the Read/Write Bit for Slave Address									
Protocol Analyzer Colo	(
Start	Data	Slave Addr	Read	Write	Reg	Addr					
		***				***					
A-ACK.	A-NACK	D-ACK	D-NACK.	Stop							

Fig 4-67 – Protocol Analyzer I2C Configuration dialog box

Step6. Set the I2C Configuration dialog box.

Pin Assignment:

SDA Channel: It is the Data channel, and the default is A0.

SCL Channel: It is the Clock channel, and the default is A1.

Data Mode: Set the Data Length used by the Slave Addr and the Data.

Protocol Analyzer Property:

Set the Write Bit or Read Bit to Low Level.

Set the ACK or NACK to Low Level.

Don't stop analyzing when NACK appears: When the option is selected, the data will be analyzed continuously when the NACK appears.

Add the Read/Write Bit for Slave Address: When the option is selected, the decoding will be displayed by way of the added Read/Write Bit for Slave Address.

Protocol Analyzer Color: Users can vary the colors of the decoded packet.

Step7. Press OK to exit the dialog box of Protocol Analyzer I2C.

Step8. Click Run to acquire I2C signal from the tested I2C circuit. Refer to Fig 4-68.

Tip: Click 📓 icon to view all data, and then select the waveform analysis tools to analyze the waveforms.

	KTEADDANA		Dealer	28.12845 € S € B ₺ 5 2 £ 4 mm (B + 15 * 1980) 24 • Tappe Deep (Them) Prov 28.42865 au A Prov 5 2000 mm * A 1 * 5 2000 mm * A 3 * km * Regel 214212m * 1 8 Prov 12 2000 mm * 8 1 * 6 2000 mm * Competition (Pr. 80)
			1.000	And the Bringhouse and the Bringhouse and
			1 1	KOPES DO MIN (AND DATA AND
	A PARTY OF	and the second second		
			1	
				7
a				
	44.0	120	-	
				1 L L L L L L L L L L L L L L L L L L L

Fig 4-68 – Waveform Analysis



4.5.2.2 Protocol Analyzer I2C Timing Analysis

PROTOCOL ANALYZER I2C	×
Configuration Timing Packet Data Format Register	
Waveform Image SDA \rightarrow \leftarrow tsu:dat SCL thd:sta \rightarrow \leftarrow thd:sta \rightarrow \leftarrow	
Time Format Settings Image: Activate Time Settings Image: HD:STA: 0.50 to: 50.00 us Image: KSU:DAT: 0.20 to: 50.00 us Image: HD:DAT: 0.20 to: 50.00 us Image: KSU:STD: 0.50 to: 50.00 us	
OK Cancel Default H	elp

Fig 4-69 – Protocol Analyzer I2C Timing dialog box

Waveform Image: Describe the position of the set time.

Time Format Settings: When the Time Settings is activated, the set time will become the condition of judging decoding. For example, when you want to decode START, you should judge whether the conditions of START are satisfied firstly, and then judge whether the set time of tHD: STA is coincident with the factual waveform. If the two conditions are satisfied, the START can be decoded. Other segments decoding of the packet is the same with that of the START.



OTOCOL ANALYZER I		_		
Configuration Timing	Packet Data Format	Register		
lbem	Color	Item	Color	
🔽 [Slave Add]	***	ANACK		
P Read		D-ACK		
₩ Write		D-NACK		
I⊄ Data	**	P Describe		
A-ACK		🔽 Reg Addr	11	
		ОК	Cancel Default	Не

4.5.2.3 Protocol Analyzer I2C Packet Analysis

Fig4-70 - Protocol Analyzer I2C Packet dialog box

In the Packet dialog box, users can select the set item to be displayed and the color of item. It is a Bus Packet List view, which includes 4 formats, which I2C happens as follows.

acket #	Name Bus1(I2C)	TimeStamp -1us	ADDRESS S0	Write	A-ACK A-ACK	00	D-ACK	75	D-ACK	01	D-ACK	23	D-ACK	45	D-ACK
6 acket #	Name	TimeStamp	ADDRESS	Write	A-ACK	DATA	DHACK	DATA	D+ACK						
2	Bus1(I2C)	10.2064ms	50	Write	A-ACK	00	D-ACK	75	D-ACK						
acket #	Name	TimeStamp	ADDRESS	Read	A+ACK	DATA	D-NACK	DESC	RIBE						
3	Bus1(I2C)	10.2982ms	50	Read	A-ACK	01	D-NACK	DATA	NACK						
acket #	Name	TimeStamp	ADDRESS	Read	A-ACK	DATA	D-AUK	DATA	D+AOK	DATAS	DAMOR	DESC	RIBE		
4	Bus1(I2C)	10.3554ms	50	Read	A-ACK	23	D-ACK	45	D-ACK	67	D-NACK	DATAN	VACK		
acket #	Name	TimeStamp	ADDRESS	White	A-ACK	DATA	DHACK	DATA	DHADE	DATA	DHU	DATA	EDHALK	DATA	0-1105
5	Bas1(I2C)	20.477ms	50.	Writer	A-ACK	00	D-ACK	79	D-ACK	89	D-ACK	AB	D-ACK	CD	D-ACK
5	Bus1(I2C)	20.477ms	50.	Writer	A-ACK	00	D-ACK	79	D-ACK	89	D-ACK	AB	D-ACK	CD	D-AC

Fig4-71 - Protocol Analyzer I2C Packet List

Packet1: It is commonly normal data, which includes 1 "Address" and 6 "Data".
Packet2: It is commonly normal data, which includes 1 "Address" and 6 "Data".
Packet3: It is commonly normal data, which includes 1 "Address" and 14 "Data".
Packet4: It is commonly normal data, which includes 1 "Address" and 6 "Data".
Packet4: It is commonly normal data, which includes 1 "Address" and 6 "Data".

When judging the start of I2C, it is the Packet TimeStamp.

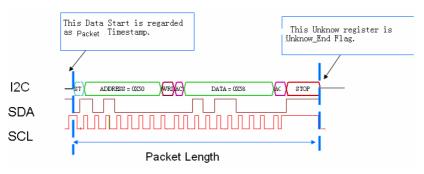


Fig4-72- Packet Length

Packet Length: From START (Start's TimeStamp) to STOP (Unknow_End Flag TimeStamp).



Packet Idling Length: From Unknow_End Flag TimeStamp to Start's TimeStamp.

This Unknow register is Unknow_End Flag.

4.5.2.4 Protocol Analyzer I2C Data Format Analysis

P	PROTOCOL ANALYZER 12C										
	Configuration Timing Pa	acket Data Fo	rmat Register								
	Activate										
	Data:	C Binary	C Decimal	Hexadecimal	C ASCII						
	Slave Addr:	C Binary	C Decimal	Hexadecimal							
	Reg Addr:	C Binary	C Decimal	Hexadecimal	C ASCII						
				OK Can	cel Default	Help					

Fig4-73- Protocol Analyzer I2C Data Format dialog box

Users can set the Data Format of the Data, Slave Addr and Reg Addr as their requirements. When selecting the option, Activate, the data formats are decided by the settings in the Protocol Analyzer; when not selecting the option, Activate, the data formats are decided by the settings in the main program.

4.5.3 UART Analysis

UART Introduction

The UART, which stands for Universal Asynchronous Receiver/Transmitter, is a serial asynchronous protocol. The UART is often time-integrated into PC communication devices, and it usually equips an EEPROM (Electronic Erasable/Programmable Read Only Memory) for error checking proposes with other chips. There are two concepts about UART which must be understood before performing any further tasks.

The UART protocol will first translate a parallel data into serial data, for the UART requiring only one wire to transmit signals. The transmission starts at a triggered Low position, and there are 7 or 8 bits of data following afterwards. To halt a transmission, it requires a signal or multiple bits of logic '1'. Odd number bit transmission requires odd parity error checking, and even number bit transmission requires even number error checking. Following the parity check is another data translation from serial data to parallel data. UART also generates an extra signal to indicate receiving and transmitting conditions.

Furthermore, since UART is an asynchronous communication protocol and data transmission may not be in bytes, a complete UART signal Packet must consist of **Start**, **Data**, **Parity**, **Stop**, **Baud** and **TXD** segments. They are as following:

Start: When TXD is changing from HIGH to LOW voltage (1 bit).

Data: Users must decide the size of signal Packet segment from 4 to 8bits.

Parity: This performs three types of parity checks: odd parity, even parity, and none parity.

Stop: This occurs when TXD is at high voltage. This is adjustable; this is commonly set to 1 or 2.

Baud: This is the data transmission speed according to the initial condition of START.

TXD: This is the transmission direction. It is MSB \rightarrow LSB by default.



4.5.3.1 Software Basic Setup of Protocol Analyzer UART

- **Step1.** Set up RAM Size, Frequency, Trigger Level and Trigger Position as described in Section 4.1. (Tip: The Setup of the Frequency should be higher, but not too far away from the Baud Rate of the test board).
- **Step2.** Set up Either Edge as the trigger condition on the signals which are connected to the Tx pin or the Rx pin of the tested UART board.
- **Step3.** Set up the Protocol Analyzer UART dialog box. The Protocol Analyzer UART dialog box is set as the steps of I2C.

PRO'	TOCOL ANALY	ZER UART						X
Co	nfiguration Pa	cket Data For	mat F	Register				
[– Pin Assignmer	ıt						1
	Channel:	AO	•					
	- Protocol Analy	zer Property-						
	Parity Check:	None Parity	•	Data Length:	8 💌	Baud Rate:	9600 🔽 🗆 Auto	
	Stop Bit:	1	•	Percentage Sample:	70% 💌	(Min:1bps, N	Max:10Mbps)	
	Transmission Direction:	LSB->MSB	•	🗖 Data Re	everse Decoding			
[- Protocol Analy	zer Color						
		Start				Data		
		Parity				Stop		
					ОК	Cancel	Default Help	

Fig 4-74 – Protocol Analyzer UART Configuration dialog box

Step4. Set the UART Configuration dialog box

Pin Assignment:

UART only needs one channel to decode the signals, the default is A0.

Protocol Analyzer Property:

Parity Check: There are three options on the dropdown menu: None Parity, Odd Parity and Even Parity, and the default is None Parity.

Data Length: Set the Data Length in the range from 1 to 56.

Stop Bit: Select the Stop Bit from the three options: 1, 1.5 and 2, and it is stopped in the High Level. **Percentage Sample**: Users can select the Percentage from the options (50%, 60%, 70%, 80% and 90%) on the dropdown menu, and the default is 70%.

Bus/Signal	Trigger	Filter	-20 -20 -10 -5 -
Bus1 (UART)	•		(0XAA) Data : 0XAA) Data : 0XAA / Data : 0X55
● A0 A0			
🥑 A1 A1			
🥑 A2 A2			
U M2 M2			
-			
Bus/Signal		Filter	
-			
Bus/Signal	Trigger	Filter	<u> </u>
Bus/Signal Bus1 (UART)	Trigger	Filter	<u> </u>

Transmission Direction: Set the Transmission Direction to MSB->LSB or LSB->MSB.

Fig 4-75 – Data Waveforms MSB->LSB and LSB->MSB

Baud Rate: The dropdown menu has options as below: 110, 300, 600, 1200, 2400, 4800, 9600, 19200,



38400, 57600, 115200, 230400, 460800 and 921600. Users can select the desired value from the menu. At the same time, The **Auto** can be selected to calculate the Baud Rate automatically (If the Auto is selected, the Baud Rate will be calculated and displayed on the Configuration dialog box automatically.).

Data Reverse Decoding: When the option is selected, the data will be decoded in reverse.

Bus/Signal	Trigger	Filter	-20	-15	-10	-5		5	10	15
Bus1 (UART)			Unknow	Start			Data	OXAA		K
• A0 A0	X -						أــــــــــــــــــــــــــــــــــــ			Ĺ

Without using the reverse data level to decode

Bus/Signal	Trigger	Filter	5		-20	-15	-10	 -5	, , , ,	5	11		15	20	25
Bus1 (UART)		\times		Inknow	Start	(Data : 0XA	A			Data : 0X	AA		
● A0 A0	Х -			ĺ		Í					1		1		Ē

Using the reverse data level to decode

Fig 4-76 – Without/With the Reverse Data Level for Decoding

Protocol Analyzer Color:

Users can vary the colors of the decoded packet.

Step5. Press OK to exit the dialog box of Protocol Analyzer UART.

Step6. Click Run to acquire the UART signal from the tested UART circuit. Refer to Fig 4-77.

Tip: Click 📓 icon to view all data, and then select the waveform analysis tools to analyze the waveforms.

2 1 2 2 4 1		Omplay	Image 20 005551ma A Fac 161 71651ma A T + ET 71051ma A - T + ET 71051ma A - T + ET 71051ma Image 20 005551ma A Fac 161 71651ma A - T + ET 71051ma A - T + ET 71051ma Compare Tables 35.723
Incorport	1100	149	and the second data and the second
Bari (GMIT)		0	Start Data 0407 Start Data 0402
●A6 40	×	0	
		-	
 Al At 	100	0	
14 FA		0	
# 24 -5+	1.24		
✓ A5 (41)	. 20	σ	
¥ 86 -51	小型三	一位	
8 42 ST		0	
# 80 10	50	一級	
■ 11	20	0	
# 82 .10	1.002	一些	
• B3 111	386	0	
# 84 14	计理由	- R.	
* #5 ==	.32	(0)	
# 85 10	1361	100	
# 17 11	1413	0	
🖌 CB (18	1280	- 10-	
e G ()	32	0	
4 q	1200	一個	
- a a	2891	0	

Fig 4-77 – Waveform Analysis



4.5.3.2 Protocol Analyzer UART Packet Analysis

PROTOCOL A	NALYZER UART						×
Configuratio	n Packet Data	Format Register	1				
	Item	Color		Item	Color		
	🔽 Data			🔽 Parity			
	🔽 Describe						
_							
	Packet Idle(T	ime)	5ms	(Min:10ns,	Max:10s)		
			← Time →				
	- Data:	OXC2	UNKNOW	Data: OX62	UNKN	WΟ	
L							
			OK	Cano	cel Default	:	Help

Fig4-78 - Protocol Analyzer UART Packet dialog box

Data: List Data field captured by Bus in the packet display.

Parity: Display parity check in packet.

Describe: Error description to any field (format or data bit).

Packet Idle (Time): When the check box is selected, the default value is 5ms. Specifically, when the Packet Idle (Time) is activated, the packet will be divided again according to the Packet Idle (Time). If the Time Length between the previous packet and the next packet is more than 5ms, the two packets will still be divided, or the two packets will be merged into one packet.

It is a Bus Packet List view, which includes 4 formats, which UART happens below. PARITY clews whether users start PARITY or not.

tting	ist Refresh Export	Synch Para	ameter]		_
Packet #	Name	TimeStamp	Data	Parit	γ	
1	Bus1(UART)	-21927	86	Even Parif	ty .	
Packet #	Name	TimeStamp	Data	Parity		DESCRIBE
2	Bus1(UART)	81164	6C	Error-0	Parit	y Error, should Low
Packet #	Name	TimeStamp	Data	Parit	Y	
3	Bus1(UART)	184247	D9	Even Parit	ly .	
Packet #	Name	TimeStamp	Data	Parit	Y	1
4	Bus1(UART)	307617	EC	Even Parit	ίγ.	

Fig4-79 - UART Packet List

Packet1: It is commonly normal Data, which includes 1 "Data" and 1 "Parity"; its parity is Even Parity. **Packet2:** It is the state of Parity Error; the DESCRIBE is "Parity Error, should Low ".

Note: Because the Even Parity and the Odd are impossible to present to the same Bus, so we only take the Even Parity for an example here.

Packet3: It is commonly normal Data, which includes 1 "Data" and 1 "Parity"; its parity is Even Parity.



Packet4: It is commonly normal Data, which includes 1 "Data" and 1 "Parity"; its parity is Even Parity. Packet Length: When judging to the start of UART, it is the packet TimeStamp.

State 1: Having Stop:

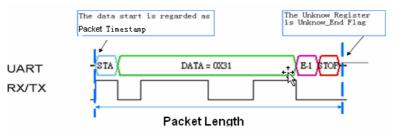


Fig4-80 - Packet Length

State 2: No Stop:

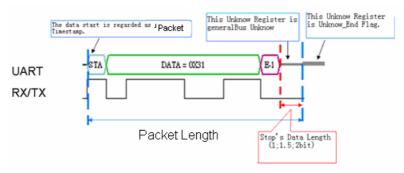


Fig4-81 - Packet Length

If the STOP falls short of condition, it isn't noted down in UART.

Packet Length: From START (Start's TimeStamp) to STOP (Unknow_End Flag TimeStamp)

Packet Idling Length: Unknow_ End Flag TimeStamp to START TimeStamp.

4.5.4 **SPI** Analysis

SPI Introduction

SPI (Synchronous Peripheral Interface) is a parallel synchronous full duplex protocol with a Bus-like physical interface. This protocol was first developed by Motorola and was generally used for EEPROM, ADC, FRAM, and display device drivers which are equipped with low data transmission speed. The SPI data transmission is synchronous in both receiving and transmitting directions. Although Motorola initially did not define the clocking impulse, it is commonly seen that the clocking impulse is according to the master processor. In practice, there are two clocking impulses: CPOL (Clock Polarity) and CPHA (Clock Phase). The configuration of both CPOL and CPHA decides the sampling rate. When the SPI must transmit serial data, it initiates the highest bit.

Since SPI is a synchronous communication protocol and data transmission may not be in bytes, a complete SPI signal Packet must consist of SCK, MOSI, MISO, and SS segments with CPHA and CPOL. They are as following.

SCK: Serial Clock Line (SCL).

MOSI: Master data output, Slave data input (MOSI stands for Master-Out-Slave-In).

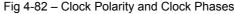
MISO: Master data input, Slave data output (MISO stands for Master-In-Slave-Out).

SS: SS stands for Signal Selector of the master device which is to select signals for the Slave devices.

CPHA: The clock phase (CPHA) control bit selects one of the two fundamentally different transfer formats.

CPOL: The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock.

The grant stre stream the strengthest	The data are driven and sampled
Clock Polarity = 0 where rising edges happen Clock Phase = 0 where wave cycle start	Clock Polarity = 0 where rising edges happen Clock Phase = 1 where wave cycle end
The data and driven and sampled	Bue data are driven and sampled
Clock Polarity = 1 where rising edges happen Clock Phase = 0 where wave cycle start	Clock Polarity = 1 where rising edges happen Clock Phase =1 where wave cycle end
Fig 4-82 – Clock Pola	arity and Clock Phases





4.5.4.1 Software Basic Setup of Protocol Analyzer SPI

- Step1. Set up RAM Size, Frequency, Trigger Level and Trigger Position as described in Section 4.1.
- Step2. Set up the Falling Edge on the signal of SS which connected to the Signal Selector (SS) pin of the SPI tested board.
- Step3. Set up the Protocol Analyzer SPI dialog box, the Protocol Analyzer SPI dialog box is set as the steps of I2C.

PROTOCOL ANALYZER SPI	2	×
Configuration Packet Data Format Register		
Pin Assignment SCLK: ▲0 DATA: A1 Protocol Analyzer Property Mode: CPHA=0,CPOL=0 ▼ Transmission MSB->LSB ▼ Direction: MSB->LSB ▼ Data Length: 8 bit Fill*0" at the LSB when the bit count is not enough.	SS Pin Assignment SS Channel SS Channel: A0 SS Setting: Cow C Virtual SS Idling Time: 20ns (Mir:20ns Max1.311ms) C Don't care data bit	
Protocol Analyzer Color		
Data		
ОК	Cancel Default Help	

Fig 4-83 – Protocol Analyzer SPI Configuration dialog box

Step4. Set the SPI Configuration dialog box

Pin Assignment:

SCLK: It is the Clock channel, and the default is A0. **DATA:** It is the Data channel, and the default is A2.

Protocol Analyzer Property:

Mode:

There are six modes for selecting, which are CPHA=0,CPOL=0; CPHA=1,CPOL=1; CPHA=1, CPOL=0; CPHA=0, CPOL=1; Rising and Falling. **Transmission Direction:** Set the Transmission Direction to MSB->LSB or LSB->MSB. **Data Length:** Set the Data Length in the range from 1 to 56, and the default is 8.

Fill "0" at the LSB when the bit count is not enough: For example, the value of Data is "1001111", there is only 7 Bits. When the value of Data is set to 8 Bits, the displayed value should be 10011110.

SS Pin Assignment:

SS Channel: Select the channel for the SS, the default is A1.

SS Setting: Set the Judgment Level of the SS Channel to Low or High.

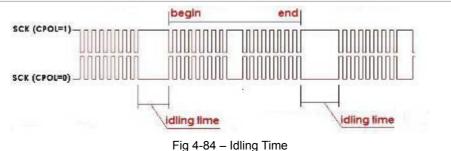
Virtual SS: When the SS Channel is not activated, the Virtual SS will be activated. The Idling Time of the

Virtual SS should be set as an auxiliary condition to decode.

Type the idling time of the SCLK signal on the tested SPI circuit. The idling time is defined as the idling

time as shown in Fig 4-86.





Protocol Analyzer Color: Users can vary the colors of the decoded packet.

Step5. Click OK to exit the dialog box of Protocol Analyzer SPI.

Step6. Click Run to acquire the SPI signal from the tested SPI circuit. Refer to the Fig 4-87.

Tip: Click icon to view all the data, and then select the waveform analysis tools to analyze the waveforms.

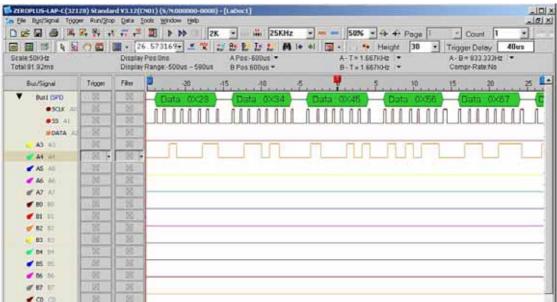


Fig 4-85 – SPI Signal



4.5.4.2 Protocol Analyzer SPI Packet Analysis

P	ROTOCOL ANAI	LYZER SPI				×
	Configuration	Packet Data Forma	t Register			
	Item	Color				
	🔽 Data					
			OK	Cancel	Default	Help

Fig4-86 - Protocol Analyzer SPI Packet dialog box

DATA: List Data field captured by Bus in the packet display.

BUS Packet List:

1 Bust(SPI) 57 12 23 34 45 56 67 78 89 9A det # Name TimeStamp Data Dota Data Data	Name TimeStamp Data Data	adiet #	Name	TimeStamp	Data								
2 Bus1(SPI) 415 12 23 34 45 56 67 78 09 9A deet # Name TimeGtamp Data Data Data Data Data Data	Bust(SPI) 415 12 23 34 45 56 67 70 09 9A Name TimeStamp Data	1				_							
cket # Name TimeStamp Data Data Data Data Data Data	Name TimeStamp Data Data Data Data Data Data												
		-									70	09	94
	Bus1(SPI) 774 12 23 34 44 AC CE												
3 Dus1(SPI) 774 12 23 34 44 AC CE		3	Bus1(SPI)	774	12	20	34	44	AÇ	CE	j.		

Fig4-87 - Protocol Analyzer SPI Packet List

Packet Length and Packet Idling Length

1. SS channel is activated

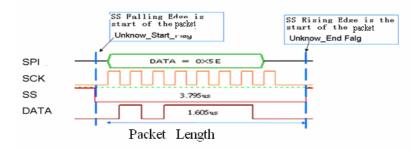


Fig4-88 - Packet Length

Packet Length: From Unknow_Start_Flag TimeStamp to Unknow_ End Flag TimeStamp

Packet Idling Length: From Unknow_End Flag TimeStamp to Unknow_Start_Flag TimeStamp

2. SS channel is not activated.



Virtual SS is activated 1: Data needs 8-bit; the Idling Time is set as 3us.

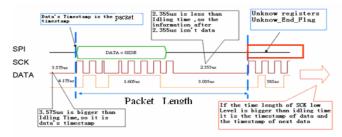
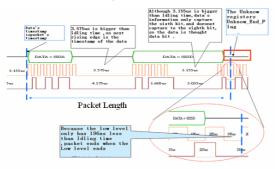


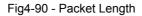
Fig4-89 - Packet Length

Packet Length: From Unknow_Start_Flag TimeStamp to Unknow_ End Flag TimeStamp

Packet Idling Length: From Unknow_End Flag TimeStamp to Unknow_Start_Flag TimeStamp

Virtual SS is activated 2: Data needs 8-bit; the Idling Time is set as 3us. Don't care data bit is not activated.





Packet Length: From Unknow_Start_Flag TimeStamp to Unknow_End Flag TimeStamp

Packet Idling Length: From Unknow_End Flag TimeStamp to Unknow_Start_Flag TimeStamp

Virtual SS is activated 3: Data needs 8-bit; the Idling Time is set as 3us. Don't care data bit is activated.

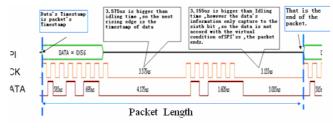


Fig4-91 - Packet Length

Packet Length: From Packet's TimeStamp Data to next Packet's TimeStamp Data

Packet Idling Length : It is 0.

The End dot is Unknown.

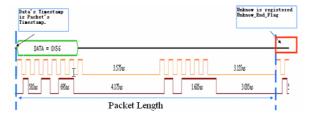


Fig4-92 - Packet Length

Packet Length: From Packet's TimeStamp Data to next Packet's TimeStamp Data Packet Idling Length: It is 0.



4.5.5 1-WIRE Analysis

Preface

To increase the Protocol Analyzer feature in order to analyze the Protocol Analyzer 1-WIRE transmission protocol data. Using LA analysis function, the required serial data can be converted and presented in the form of Bus. Therefore, the software needs to add a dialog box so as to set up a Protocol Analyzer 1-WIRE dialog box.

1-WIRE Introduction

1. Brief Introduction

Features

1-WIRE is a non-synchronic half-duplex serial transmission, which requires only one OWIO to transmit data. The typical 1-WIRE transmission structure is illustrated in Figure 4-95. During the 1-WIRE transmission, the OWIO can be used to transmit data and supply power to all devices connected to the 1-WIRE. OWIO will link to a 4.7K Ohm Pull-High electric resistance which is linked to the power supply (3V-5.5V). The transmission speed for 1-WIRE can be divided into two types, standard and high speed. Every 1-WIRE has a unique 64-bit code for the device to recognize. Therefore, the maximum number of link devices is 1.8; almost unlimited.

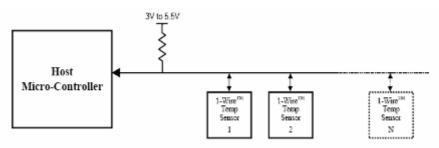


Fig4-93 - Applications

Applications

1-WIRE is commonly applied to the EEPROM and to certain sensor interfaces.

2. Protocol Analyzer Signal Specifications

Parameter	Value					
Name of Protocol Analyzer	1-WIRE					
Required No. of Channels	1					
Signal Frequency	Not fixed, around 10K					
Appropriate Sampling Rate	1MHz					
Same Data Time Per Bit	⊡Yes ■No					
Name of Syn. Signals	OWIO					
Data Verification Point	30 us after the falling edge signals					

3. Protocol Analyzer IO Description

Name	Function			
OWIO	The only I/O transmits Reset signals and data.			

4. Protocol Analyzer Electrical Specifications

Parameter	Min.	Тур.	Max.	Unit	Note
High-count Voltage	2.8		5.2	V	Every IC varies according to the Pull-High voltage.
Low-count Voltage		0		V	



Protocol Analyzer 1-WIRE Format Description

Two speed types of 1-WIRE: Standard: 1MHz (1us) High: 5MHz (0.2us) Four types of 1-WIRE Signals:

- 1. Reset:
 - Every communications period starts with Reset signal. Master will send a Reset Pulse so that all the Slave devices on the 1-WIRE Protocol Analyzer enter into recognition status. When one or many Slaves receive Reset Pulse, a Presence Pulse signal will be sent back from Slave, indicating receipt of the signal.
- 2. Write 0: Send a "0" bit to Slave (Write 1 time slot).
- 3. Write 1: Send a "1" bit to Slave (Write 1 time slot).
- 4. Read Data:

"Read data sequences" resembles "Write time slot." However, when Master releases BUS and reads data from Slave devices, Master creates samples from BUS status. In this way, Master can read any 0 or 1 bit from Slave devices.

Four signal types are described respectively in the following:

- 1. Reset:
 - (1) When Master starts communicating with Slave, Master first sends a low-count Reset Pulse (TX)



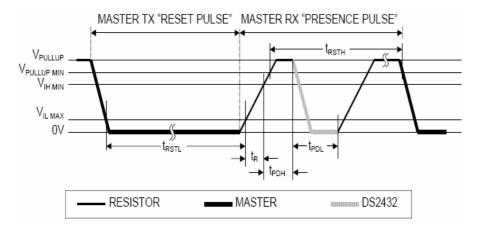


Fig4-94 - Master TX Reset Pulse and Master RX Presence Pulse

- (2) Then, Master releases Protocol Analyzer and enters the RX mode. Through high- pull resistor,1-WIRE Protocol Analyzer is pulled back to the high status.
- (3) Then, Master detects a rising edge from the Data Line when every slave will wait for a period of time (t_{PDH}^{PDH}) (standard speed: 15-60us; high speed: 2-6us) and send back a Presence Pulse to Master (t_{PDL}^{PDL})(standard speed:60-240us; high speed: 8-24us).
- (4) Finally, the 1-WIRE Protocol Analyzer will be pulled back to the high status through the resistor.
- (5) Meanwhile, Master can detect any online Slave.
- (6) From Fig4-95, the low count Reset Pulse and Presence Pulse signals can be clearly seen.



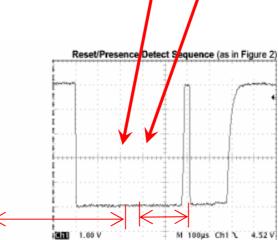


Figure 2a. You can clearly see the negative going reset and the presence pulse

Fig4-95 - Reset/Presence Detect Sequence

- 2. Write Data:
 - (1) To initialize Write Data, Master will convert the Data Line from the high logic to the low.
 - (2) There are two types of Write time slot: Write 1 time slot and Write 0 time slot.
 - (3) During a write cycle, all Write time slots must have duration of at least 60us and a recovery period of 1us.
 - (4) When the I/O line goes down, Slave devices create samples from 15-60 us.
 - A. Write 0: If the sampling is low, 0 is generated as in Fig4-98:



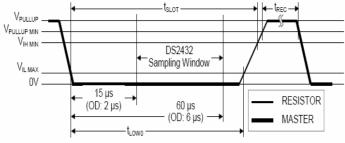


Fig4-96 - Write-zero Time Slot

B. Write 1: If the sampling is high, 1 is generated (Note: Read 1 is of a similar waveform pattern) as in Fig4-99:

Write-one Time Slot

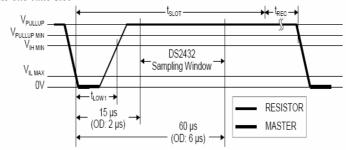


Fig4-97 - Wrote-one Time Slot

3. Read Data:

- (1) When Slave reads data, Master will generate a Read time slot.
- (2) To initialize Read Data, Master has to convert Data line from the high logic to the low.
- (3) Data line must be kept as low as 1us.
- (4) The Output Data of Slave must be 14us at most.
- (5) To read from 15us where Read slot starts, Master must stop driving I/O.
 - Read-data Time Slot

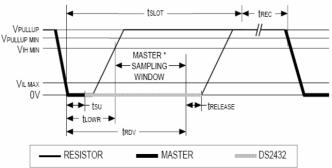


Fig4-98 - Read-data Time Slot

- (6) When Read Time Slot ends, I/O Pin will be pulled back to the high count through the external resistor.
- (7) During a write cycle, all Write time slots must have duration of at least 60us and a recovery period of 1us.
- 4. Typical 1-WIRE Conversation model can be summarized as below:

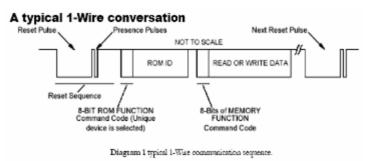


Fig4-99 - A Typical 1-WIRE Conversion

- (1) Master keeps Protocol Analyzer at low signal (standard speed: 480us; high speed: 48us) as the Reset Pulse.
- (2) Then, Master releases Protocol Analyzer and locates a Presence Pulse responded by any online Slave.
- (3) The above two points are Reset Pulse and Presence Pulse, which can be put together as a Reset Sequence.
- (4) If Presence Pulse is detected, the slave location will enable Master to access Slave using the Write 0 or Write 1 Sequence.



- 5. 1-WIRE Serial Number:
 - (1) Every 1-WIRE Slave has a unique laser memory.
 - (2) The serial number is 64bits.
 - (3) The serial numbers are 8bytes in total, located in three individual, which are illustrated as below:

MSB		nber		LSB		
8-bit	CRC		48-bit Serial Number		8-bit Far	nily Code
MSB	LSB	MSB		LSB	MSB	LSB

- (4) Starting from LSB, the first byte is for family code, which is used to identify product categories.
- (5) Next, the 48bits is the only address for storage.
- (6) The last byte, MSB is used to store CRC.



4.5.5.1 Software Basic Setup of Protocol Analyzer 1-WIRE

PROTOCOL ANALYZER 1-WIRE	×
Configuration Packet Data Format Register	
Pin Assignment	Protocol Analyzer Color
0WI0:	Reset Pulse
Protocol Analyzer Property	Presence Pulse
Connect Speed: Standard(1 us)	Data 🗾 😳
Transmission MSB->LSB	Sampling Position
Data Length: 8 bit	30 us
(Min:1bit,Max:32bit)	(Min:1,Max:120)
OK	Cancel Default Help

Fig4-100 - Protocol Analyzer 1-WIRE Configuration dialog box

Set the 1-WIRE Configuration dialog box.

Pin Assignment:

1-WIRE only needs one channel to decode the signals, and the default is A0.

Connect Speed:

The Connect Speed can be set to Standard(1 us) or High(0.2 us).

Transmission Direction:

The Transmission Direction can be set to MSB->LSB or LSB->MSB.

MSB->LSB: From High Level to Low Level.

LSB->MSB: From Low Level to High Level.

Data Length:

The Data Length can be set in the range from 1 to 32-bit, and the default is 8-bit.

Sampling Position:

The Sampling Position can be set in the range from 1 to 120us, and the default is 30us.

Protocol Analyzer Color:

Users can vary the colors of the decoded packet.



User Interface Instructions

Set up the Protocol Analyzer 1-WIRE dialog box which is set as the steps of I2C.

PROTOCOL ANALYZER 1-WIRE											
Configuration Packet Data Format Register											
Pin Assignment	Protocol Analyzer Color										
0W10: 🛛 🖊	Reset Pulse										
Protocol Analyzer Property	Presence Pulse										
Connect Speed: Standard(1 us)	Data 🗾 😳										
Transmission MSB->LSB	Sampling Position										
Data Length: 8 bit	30 us 300 us										
(Min:1bit,Max:32bit)	(Min:1,Max:120)										
ОК	Cancel Default Help										

Fig4-101 - Protocol Analyzer 1-WIRE Configuration dialog box

STEP 1. Select Channel

1-WIRE has only one OWIO. Select the channel that it is to link the OWIO.

PROTOCOL ANALYZER 1-WIRE	×
Configuration Packet Data Format Register	
Pin Assignment	Protocol Analyzer Color
	Reset Pulse
Protocol Analyzer Property	Presence Pulse
Connect Speed: Standard(1 us)	Data
Transmission MSB->LSB	Sampling Position
Data Length: 8 bit	30 us the second
(Min:1bit,Max:32bit)	(Min:1,Max:120)
OK	Cancel Default Help

Fig4-102 - Protocol Analyzer 1-WIRE Channel Setup



STEP 2. Set the Connect Speed

1-WIRE has two modes: Standard(1 us) and High(0.2 us). The speed setup according to the specifications of the object to be tested and the default mode is standard.

PROTOCOL ANALYZER 1-WIRE	×
Configuration Packet Data Format Register	
Pin Assignment	Protocol Analyzer Color
	Reset Pulse
Protocol Analyzer Property	Presence Pulse
Connect Speed: Standard(1 us)	Data 🗾 😳
Transmission MSB->LSB	Sampling Position
Data Length: 8 bit	30 us
(Min:1bit,Max:32bit)	(Min:1,Max:120)
Ōĸ	Cancel Default Help

Fig4-103 - Protocol Analyzer 1-WIRE Connect Speed Setup

STEP 3. Set the Transmission Direction

Set the Transmission Direction as either MSB -> LSB or LSB -> MSB.

PROTOCOL ANALYZER 1-WIRE	×
Configuration Packet Data Format Register	1
Pin Assignment	Protocol Analyzer Color
0W10: A0 💌	Reset Pulse
Protocol Analyzer Property	Presence Pulse
Connect Speed: Standard(1 us)	Data
Transmission MSB->LSB	Sampling Position
Data Length: 8 bit	30 us
(Min:1bit,Max:32bit)	(Min:1,Max:120)
OK	Cancel Default Help

Fig4-104 - Protocol Analyzer 1-WIRE Transmission Direction Setup

STEP 4. Set the Sampling Position

Users can slightly adjust the sampling position of 1-WIRE. This feature is applicable when the signal cannot be decoded. The default value is 30us.



PROTOCOL ANALYZER 1-WIRE	X
Configuration Packet Data Format Register	
Pin Assignment OW10: A0	Protocol Analyzer Color Reset Pulse
Protocol Analyzer Property Connect Speed: Standard(1 us.	Presence Pulse
Transmission MSB->LSB	Sampling Position
Data Length: 8 bit (Min:1bit,Max:32bit)	30 us 4300s (Min:1,Max:120)
OK	Cancel Default Help

Fig4-105 - Protocol Analyzer 1-WIRE Sampling Position Setup

STEP 5. Set the Data Length

This function decides how many bits of data can be combined as one set of figures. The default is 8 bits, and the maximum is 32bits.

PROTOCOL ANALYZER 1-WIRE	X
Configuration Packet Data Format Register	,
Pin Assignment	Protocol Analyzer Color
0W10: A0 💌	Reset Pulse
Protocol Analyzer Property	Presence Pulse
Connect Speed: Standard(1 us)	Data
Transmission MSB->LSB	Sampling Position
Data Length: 8 bit	30 us
(Minerbic/Max.32Dit)	(Min:1,Max:120)
ОК	Cancel Default Help

Fig4-106 - Protocol Analyzer 1-WIRE Data Length Setup



4.5.5.2 Protocol Analyzer 1-WIRE Packet Analysis

PROTOCOL ANALYZER 1-W	VIRE	×
Configuration Packet D.	ata Format Register	
Item	Color	
🔽 Data		
🔽 Describe	•	
	OK Cancel Default	Help

Fig4-107- Protocol Analyzer 1-WIRE Packet dialog box

That is the new View; the below View includes several formats that 1-WIRE can happen; it describes Data number and their positions.

ietting	Refresh Export	Synch Parame	ster	<u> </u>																
Packet #	Name	TimeStamp									Dat)								
1	Bus1(1-WIRE)	4032363	30	96	30	96	03	90	02	40	87	FF	Æ	FF	FF	FF	FF	04	00	
Packet #	Name	TimeStamp									Dat	3								
2	Bus1(1-WIRE)	8065053	30	96	30	96	07	90	00	40	F7	FF	Æ	Æ	FF.	FF.	FF	04	00	
Packet #	Name	TimeStamp		_	_	_	_	_	_		Dat		_	_	_	_	_	_		
3	Bus1(1-WIRE)	12096936	33	96	30	96	03	90	02	48	ЗF	FF	FF	FF	FF	FF	FF	04	00	
Packet #	Name	TimeStamp		_	_	_	_	_	_		Dati	•	_	_	_	_	_	_		
4	Bus1(1-WIRE)	16129232	33	96	30	96	03	90	02	48	ЗF	FF	FF	FF	FF	FF	FF	04	00	
Packet #	Name	TimeStamp									Dat)								
5	Bus1(1-WIRE)	20161527	33	96	30	96	07	90	01	40	2	FF	FF	FF	FF	FF	FF	04	00	

Fig4-108 - Protocol Analyzer 1-WIRE Packet List

Packet 1: It is commonly normal Data, which includes 1 "Data".
Packet 2: It is commonly normal Data, which includes 1 "Data".
Packet 3: It is commonly normal Data, which includes 1 "Data".
Packet 4: It is commonly normal Data, which includes 1 "Data".
Packet 5: It is commonly normal Data, which includes 1 "Data".
Packet 5: It is commonly normal Data, which includes 1 "Data".



4.5.6 HDQ Analysis

Preface

Increase the Protocol Analyzer feature to analyze the Protocol Analyzer HDQ transmission protocol data. Using LA analysis function, the required serial data can be converted and presented in the form of Protocol Analyzer. Therefore, the software needs to add a dialog box so as to set up a Protocol Analyzer HDQ dialog box.

HDQ Introduction

1. Brief Introduction

Features

Protocol Analyzer HDQ is a non-synchronic half-duplex serial transmission, which requires only one HDQ and uses a quasi-PWM (Pulse Width Modulation) to verify the serial data.

Applications

HDQ is commonly applied to the display interface for battery management.

2. Protocol Analyzer Signal Specifications

Parameter	Value
Name of Protocol Analyzer	HDQ
Required No. of Channels	1
Signal Frequency	Not fixed, around 12MHz, 13MHz and 19,2MHz
Appropriate Sampling Rate	100MHz
Same Data Time Per Bit	□Yes ■No
Name of Syn. Signals	HDQ
Data Verification Point	Low signals $>$ 190us converts to High signals $>$ 40us

3. Protocol Analyzer IO Description

Name	Function
HDQ	The sole I/O transmits Host and BQ-HDQ status and data.

4. Protocol Analyzer Electrical Specifications

Parameter	Min.	Туре	Max.	Unit	Note
Logic Input High	2.5			V	
Logic Input Low			0.5	V	

Protocol Analyzer HDQ Format Description

The format changes according to the pulse width, so the display must refer to the defined pulse width. Protocol Analyzer HDQ is made up of 16 bits signals. Firstly, after the period of status signals, a device will be installed for the 7 bits address through the Host so that 1-bit signals can be read or written. After a response time of high signals, data will be exported in 8 bits format with the data and location content from LSB to MSB. The following is the Host to BQ-HDQ analysis.



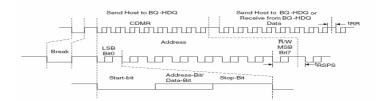


Fig4-109 - Host to BQ-HDQ Analysis

Protocol Analyzer Format

Break

This is the initial bit for the Protocol Analyzer HDQ: after Low signal lasting a period of t (B), it is then converted to a High signal lasting a period of t(BR). The length of Low signal is no less than 190us whereas the High signal is no less than 40us.



Fig4-110 - Pulse from Low to High

Address

The Address comprises 7 bits. The initial Low signal lasts a period of t(HW1) and if the write-0 status continues through the end of the t(HW0) period, the signal will convert to High and last throughout the period of t(CYCH), as shown by the dotted line in the following figure. Conversely, if it is the write-1 status, after t(HW1) period of time, the signal will convert to High and last throughout the period of t(CYCH), which is of 1 bit and no less than 190 us. The t(HW1) range is from 0.5us to 17us and no more than 50us. The t(HW0) range is from 86us to 100us and no more than 145us.

Read/Write

Read/Write is 1 bit. 0 and 1 are displayed in the same way as the above description.

T (RSPS)

The High signal lasts a period of 190us-320us. The following 8-bit data is Send Host to BQ-HDQ or Receive from BQ-HDQ Data.

Data

Made up by 8 bits, and it is Send Host to BQ-HDQ or Receive from BQ-HDQ Data. It operates in the same way as in 2.2 and the data is from LSB to MSB.

BQ-HDQ To Host

If the data transmission is read by BQ-HDQ To Host, the initial Low signal lasts a period of t(DW1) and if the write-0 status continues through to the end of the t(DW1) period, the signal will convert to high and last throughout the period of t(CYCD), as shown by the dotted line in the following figure. Conversely, if it is the write-1 status, after t(DW1) period of time, the signal will rise and last throughout the period of t(CYCD), which is of 1 bit and ranges from 190us to 260us. The t(DW1) ranges from 32us to 50us and no more than 50us. The t(DW0) ranges from 80us to 145us.

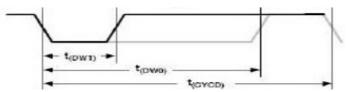


Fig4-111 - Signal from BQ-HDQ to Host



4.5.6.1 Software Basic Setup of Protocol Analyzer HDQ

PROTOCOL ANALY	ZER HDQ							×
Configuration Pa	icket Data For	mat	Register					
Pin Assignment Channel:	A0 🔽							
Time Settings(u	(s)							
Break:	190	to	1000000	Recovery:	40	to	1000000	
Host 1:	0	to	70	Device 1:	0	to	70	
Host 0:	80	to	180	Device 0:	80	to	180	
Host Bit:	190	to	260	Device Bit:	190	to	260	
Response:	190	to	320	Remark:1000	000 is infinite			
Protocol Analyz	zer Color							
Break	Recover	У	Address	Read	Write		Data	
				ок	Cancel	Defa	ult Help	

Fig4-112 - Protocol Analyzer HDQ Configuration dialog box

Set the HDQ Configuration dialog box.

Pin Assignment:

HDQ has only one signal channel, therefore it only specifies the name of the channel and marks the selected channel.

Protocol Analyzer Name: Display the name of the selected Bus.

Channel: Preset as A0.

Timing Settings(us):

Set the time for Break, Address, Read, Write, Data and Recovery.

Protocol Analyzer Color: Users can vary the colors of the decoded packet.



Operating Instructions

Open the LA operation interface.

The state of the s			and the second se	-	IIIMHz	• 50	and the second second	and an other states of the	• Count	and the second second
ale 100ms tal 254 State	ki 🚥	Display Pos Display Ran	0hs ge-2 fus - 2 Bus	A Post	1.545 *	A-7	Height 1 1 5us * 1 1 5us *	26 •	A - B = 3us Compi-Rate t	11
Bus/Signal	Tigget	fiku 📕		15ag	4ur	0-se	500 y	. he	13m	
€ A0 .==	10.4	100 -	Association and a second second	and a state of the	or deally deally dealer where the	dadate to be back	-topolatatat	distant distant	and the factor bades	
# AL AL	16	1.05								
# 32 42	H	1.22								
- A3 43	10	-36								
* M .44	8	26								
🖌 AS 45.	25	- 26.								
# 26 m	10	35								
ef 47 47	20	000								
🖋 20 👘	18	25								
# 80. 01	26	00 1								
# N2 (1)	16	26								
. 82 11	M	30								
# 24 11	100	00								
4 85 31	16	26								
# N ==	16	100								
W 87 11	10	28.								
* co =	15	10								
ea o	- 25	28.								
∉ α.α	10	35								
a a	20	000								
# CA 14	1.00	26								

Fig4-113 - Operation Interface

Sample the HDQ signal or open the sampled waveform.

	4 94 mili 14 m 0 0 li		30 >>>> >>>> 10% > +<>+ Page 1 • Count 1 • 13223m •
at 167 874075m	Sales and the second	Display Pr	05.28.440299ms A Pos. 16.770140ns A To 16.770140ms A B 1500s * Lange 8.140281ms B Pos. 16.76098ms B To 16.76098ms Compl.Ratk 255.850
Bus/Signal	Trigger	.Piter	2434165m, 120155m, 1000055m, 147045mm, 2044056m, 2156415m, 2167255m, 1750645m, 4300755m, 45000
✔ A0 .==	N -		16.775ms 191.747ma
# AL 11	16	1.00	167.674ms
# 32 42	H	-0	167 674ms
A3 43	X	2	167.574ms
# M /4	8	19	167 674ms
🖋 AS 115	×	8	167.674mi
* 36 41	15	149.5	167,674ms
ef 47 47	20	6	167.674ms
🖋 80 🐘	18	10	167.674ms
# 80. 11	15	0.1	167.674ms
ef \$2.51	N.	18	167.674ms
	X	- 19	167.674ma
# 24 14	100	-01	167.674ms
4 85 (1).	M	100	167.674ma
# N ==	15	-0-	167 674ms
W 82 11	1	2	167.674ms
* co =	15	.0	167 674ms
e a o	26	8	167.674ms
🕊 CZ. 🗇	15	- 10	167.674ms
00	20	6	167 674ms
# C8 14	100	1.00	167.674mi

Fig4-114 - HDQ Waveform



Arrange the signal channels into Bus.

Statement of the local division of the local	4 24 12 0 00		43223m +	128K - m m 200MHz - m 10N + + + Page 1 - Count 1 - 12K - m m 200MHz - m Height 25 - Tagger Delay Inn						
e 1.143223ms c187.674075m	(The second s		Pau 20.440296 Range -8 1402	Ims A Pos-16 7701 Ansi = A - T = 18.7701 Ams .= A - B = 150ns .=						
Buc/Signal	Traper	ite.	2.424	1874 1.291 Person . 30000855 m. 14.72410m. 20.440290m 26.156411m. 21.072530m. 27.550641m. 43.094757m. 49.020						
# AD 141	N .	1 .	16.775m							
	pling Setup			167.674ms						
# A2	and some re-			167.674ma						
	tog Waveform			167.674ms						
# 24 Ber				167.674ms						
✓ A1	o mi ha	á	10	167.674ms						
	out that the		10	167.674ms						
# A7 Add Channel				167.674ms						
🖌 50 Capy Channel				167.674ms						
Delete Charvel Delete Al Charcels				167.674ms						
€ Sz Res	the Defait Ch	annia		167.674ms						
	ngi Rimi			167.674m5						
# 14	ate	0	-	167 674ms						
# 85 .15	12	0		167.674ms						
# D6 11	21	. 100		167.674ms						
af \$7 10	26	- 10 -		167.674ms						
🖌 CB 10	36	7.00.0		167.674ms						
🖌 (1) (1)	10	100	1	167,674ms						
¥ a a	16	6		167 674ms						
000	20	.40		167.674ms						
- CA CA	- 102	100		157 674ms						

Fig4-115 - Group into Bus

Select Bus Property.

abe 1 143		2	Display P	Image: Status Image: S
Bue/Sg	pul .	Tagger	Do.	2.42415540 3.2919540 3.00005540 34.7247840 30.44229544 35.15641144 31.82253644 37.525544 43.32475544 43.3247554
i iii	Satulog	letar	1 - 14	TND WE DE
	(harrels)			16.775ms 131.747ms
• 13	Analist W			167.674ms
*	Dings bic			167.674ms
	Reverse			167.674ms
•	9(167.674ms
 Ungroup from But OH+U 				167.674ms
 Add Ovaread 				167.674ms
*	· Carl Charles			167.674ma
✓ Deleta Al Channels				167.674ms
	Reators D	elast Channe	•	167.674ms
	Format Ro			167.674ms
1.00	Parvane	1 12		167.674ms
2 24	10	12	不翻分	167.674ms
	£	15	0	167.674ms
ef 24.	10.	10		167.674ms
12	10	15	10	167.674ms
e ca	0	34	18	167,674ms
• a	ά i	10	0	167.674ms
* a	ä	16	10	167 674ms
	2		-	167.674ms

Fig4-116 - Bus Property

Select the decoding function of the protocol analyzer HDQ and select OK to confirm.

le 1 143223ms at 187 874075ms		Display Pr	3222mm ≤ 22 22 22 22 22 22 22 24 24 24 24 24 25 25 25 25 25 25 25 25 25 25 25 25 25
Buo/Signal	Togger	Dan P	3 4 34 100 1 70 100 1 100 100 1 1 71 100 1 1 100 100
Buil			Sus Property
	N	0	Bus Setting 131.747ms
✓ AL A)	15	10	Cha OPDAL
# A2 42	- 16	- 6 -	- Canada (and a second se
(A5 11	50	-8	Perutine
# 44.94	12	0	Protocial Analyzers Setting
# M. 45	15	0	F Protocol Analyzer Parameters Carlig
¥ 24. 11	H	0	C INFORMALIA 1-OTHE PRODULE VI. 11.00(CH01)
# 47 A	15	0	C 28F0PULS LA CANZ/08 MODULE VE 32/01(0001)
et 10	15	6	C ZEROPUJI LA LIC MODULE V2.03.03 (CHIL)
# 4111	55		C TEROPUSI LA LED PER Array MODULE VI. 00.00(0001) C TEROPUSI LA SPEMODULE VI. 13.01(0001)
# 82 10	10	0	C ZEROPUJS LA LIART MODULE V2.14.00(CNR1)
A 10 11	55	0	
# 84 24	12	0	F Unite Data Fed
* 85 11	10	10	New Protocol Reducer
• N 11	10	0	OK Cancel Help
# \$7 tr	36	0	
* a =	10	- 65	167.674ms
* a.a	16	6	167.674ms

Fig4-117 - Protocol Analyzer HDQ Setup

Complete the protocol analyzer HDQ decoding.

1 28 28 29 24 1 11 11 12 14 14 1 11 12 14 14	001	- 45	Image: Second
otat 187 674075ms		Display	Range 2.733547us - 2. D Pos-16.76993mi + B - T + 16.7693ms + Comp-Rate 255.850
Bue/Signal	Trigger	, Film 1	2 231 3785564 442 0276664 688 6477754 317 7129564 1 14595764 1 37460264 1 60026644 1 63189764 2 06657544 2 209184
Buil (PDQ)			And a second sec
•A0 /01	N	在關於	218 8644 118 3418 AD 162 304 162 169 118 AD 162 164 118 AD 490 8546 11
🖉 AL 11.	H	-0	367.674m3
₹ 42 42	10	2	167.674ms
A3 -42	8	10	167 674ms
# 44 10	20	自	167.674ms
₹ 45.45	15	100	167.674ms
🕊 A6 -01		6	167 674ms
W 42 22	16	100	167 674ms
🖋 80 💷	25	0.0	167.674ms
# 15 11	16	18	167.674ms
🖉 M2 117	M	- 10	167.674ms
80.01	10	0	167.674ms
# 84 m		に開い	167.674ms
d' 85 . 10.	16	- 0 -	167 674ms
# 54 .55	10	2	167.674ms
d' 17 11	15	.0	167 674ms
e ca	25	8	167,674ms
ea a	15	. 0	167.674ms
∉ α ⊂	20	6	167.674ms
00		1.03	167.674m8

Fig4-118- Protocol Analyzer HDQ Decoding



4.5.6.2 Protocol Analyzer HDQ Packet Analysis

PROTOCOL ANALYZER H	IDQ			×
Configuration Packet	Data Format Register			
Item	Color	Item	Color	
🔽 Break		Vrite		
Recovery		🔽 Describe		
Address				
🔽 Data				
🗹 Read				
		OK	Cancel Default	Help

Fig4-119 - Protocol Analyzer HDQ Packet dialog box

Item: Select the content which needs to display in the Packet List, which includes Break, Recovery, Address, Data, Read, Write and Describe.

Color: Set color for items which needs to display in the packet list.



4.5.7 CAN 2.0B Analysis

Preface

Add Protocol Analyzer function to analyze CAN 2.0B transport protocols data. CAN 2.0B serial transmission, there are two signal channels, CANH and CANL, which match with baud ratio judge serial data. If you want to change serial data into Bus format, you need to analyze this function with LA. a dialog box needs to be added; you should set up a Protocol Analyzer CAN 2.0B dialog box.

CAN 2.0B Introduction

1. Brief Introduction

Features

CAN 2.0B (Controller Area Network) is an Asynchronous Transmission Protocol. It costs low, sky-high use rate, far data transmission distance (10KM), very high data transmission bit (1M bit/s), sending information without appointed devices according to message frame, dependable error disposal and detection error rule, message automatism renewal after damage, and node can exit Bus function on the serious error.

Applications

CAN 2.0B is used for automotive electronics correlation systems connection.

2. Protocol Analyzer Signal Specifications

Parameter	Value
Name of Protocol Analyzer	CAN 2.0B
Required No. of Channels	1
Signal Frequency	Not fixed, around 12MHz, 13MHz and 19,2MHz
Appropriate Sampling Rate	100MHz
Same Data Time Per Bit	⊡Yes ∎No
Name of Syn. Signals	CAN 2.0B
Data Verification Point	Low signals $>$ 190us converts to High signals $>$
	40us

3. Protocol Analyzer IO Description

Name	Function
CANL	The main signal source of transmission data
CANH	Signal is opposite to the signal source of transmission data

4. Protocol Analyzer Electrical Specifications

Parameter	Min.	Туре	Max.	Unit	Note
Logic Input High	2.5			V	
Logic Input Low			0.5	V	

CAN 2.0B Frame Specification

CAN 2.0B can separate into frames as follows: Data Frame, Remote Transmit Request Frame, Error Frame, Overload Frame. Because CAN2.0B is transmitted by the format of different signals, the signal can separate into CANL and CANH, and the signal direction of CANH is opposite to that of CANL. Next we analyze CAN 2.0B signal with the standard of CANL.

Basic Data Frame

Data frame can be divided into Basic CAN and Peli CAN, Data Frame of Basic CAN transmission. As follows,



message data can be separated into Start of Frame (SOB), Arbitration Field, Control Field, Data Field, CRC Field, Ack Field, End of Frame.

Arbitration Field	Control Field	Data Field	CRC Field	Ack End of Field Frame
	88			
11 bits				

Fig4-120 - Basic Data Frame

Start of Frame

Every Start of Frame must be 0, which means asking far data to come back.

Arbitration Field

Identifier is 11bits; its function is the sequence when transmitting signal, numerical value is lower, the priority is higher, and the array is from ID-10 to ID-0, and the numerical value is not all from ID-10 to ID-4, finally RTR(Remote Transmit Request) is the judgment bit of transmission or Remote Transmit Request. When RTR=0, it denotes that the data goes out; when RTR=1, it means asking far data to come back.

Control Field

Control Field consists of 6 bytes, including Data Length Code and two Reserved Bits as Peli frame for future expansion. The transmission reserved bit must be 0. Receiver receives all bits combining 1 with 0. As the below figure, IDE and RB0 of Control Field are Reserved Bits which must be 0 and the latter 4bits are only 0-8 which denotes the data behind will transmit several bytes data.

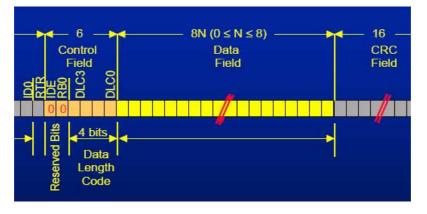


Fig4-121 - Control Field

Data Field

The Data Field consists of the data to be transferred within a Data Frame. It can contain from 0 to 8 bytes, and each contains 8 bits which are transferred MSB first.

CRC Field

16bits CRC, the last is a delimiter, and the default is 1.



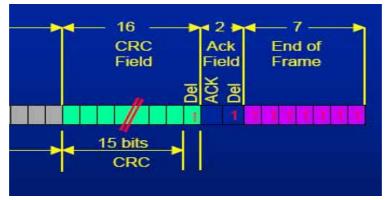


Fig4-122 - CRC Field

Ack Field

That is the return signal of Receiver, which has 2 bits, and the final is a delimiter whose default is 1. If receiving success, Ack will send back 0, then the transmitter knows the Receiver has received the data.

End of Frame

1111111 denotes en

Peli Data Frame

In the Peli Data frame, Data Frame as follows, the frame of message is separated into Start of Frame (SOB), Arbitration Field, Control Field, Data Field, CRC Field, Ack Field, End of Frame. However, the parts of Arbitration Field have much more than 18bits and the SRR and IDE are 1.

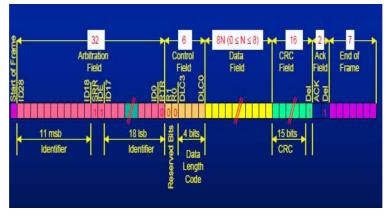


Fig4-123 - Peli Data Frame

Remote Transmit Request Frame

When RTR=1, it denotes Remote Transmit Request Frame, at this time, DLC3...DLC0 are the Data bytes of return data. And the frame doesn't have Data Field.

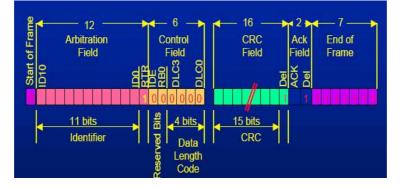


Fig4-124 - Remote Transmit Request Frame



Error Frame

The Active Error Flag consists of six consecutive Data Field 'dominant'bits. Dominant bits violate the law of bit stuffing. All bits can produce Error Frame after recognizing bit stuffing wrong, the Error Frame called Error. Corresponding Error Flag Field includes sequence bits from 6 to 12 (which produces by 1 or more nodes). Error Frame ends in Error Delimiter field. After Error Flag sends out Bus actively to get the right state, and the interrupted node tries its best to send abeyant message Error Delimiter. Error Delimiter consists of eight 'recessive' bits and allows Bus node to restart Bus transmission after Error happens.

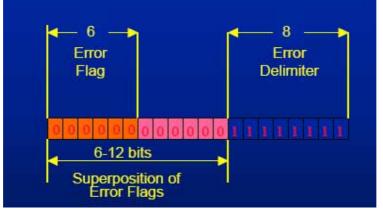


Fig4-125 - Error Frame

Overload Frame

There are two kinds of Overload conditions, which both lead to the transmission of an Overload Flag. The internal conditions of a node which require a delay of the next Data Frame start during the first bit of Intermission. Overload Flag can send six '0', which may damage Intermission format so that it makes the other nodes know node sending Overload Flag at this time. When Overload Flag is sent out, Overload Delimiter can send eight '1', others send seven '1'after finishing either.

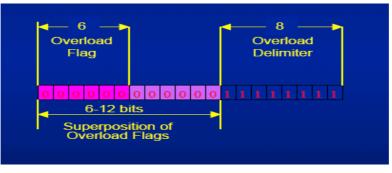


Fig4-126 - Overload Frame

Interframe Space

Interframe Space is divided into Intermission and Bus Idle. Intermission is three '1'. It is impossible to send any message during this time, except Overload Frame. The Bus is recognized to be free; the period of BUS IDLE may be of arbitrary length. And any station having something to transmit can access the Bus. When a node is at the state of 'error passive', the node will send eight '0' after INTERMISSION and other node have the chance to retransmit themselves information.



4.5.7.1 Software Basic Setup of Protocol Analyzer CAN 2.0B

PROTOCOL ANALYZER CAN 2.0B		×
Configuration Packet Data Format Register		
Pin Assignment	Start Packet Form	at
Protocol Analyzer Name: Bus1	111Bit St	art
Channel: 🗚	🔿 0 Bit Star	t
Protocol Analyzer Property		
Percentage Sample: 60% 💌 Baud Rate: 125000 💌 🗖 Auto (Min:1bps,Max:10Mbps)	 Data Reverse Decoding After End Packet happens, ju analyze When CAN Data for expansion Basic ID and ID The Del is displayd in the CR0 	n,combine
Protocol Analyzer Color Start Control C	BC Error	ACK
End ID D	ata Overload	NACK
OK	Cancel Default	Help

Fig4-127 - Protocol Analyzer CAN 2.0B Configuration dialog box

Set the CAN 2.0B Configuration dialog box

Pin Assignment: Protocol Analyzer CAN 2.0B only needs one channel to decoding signals, the default channel is A0.

Start Packet Format: The Start Position can be divided into two formats, 111 Bit Start (the Start Position is that three bits are High.) and 0 Bit Start (the Start Position is that one bit is Low).

Protocol Analyzer Property:

Percentage Sample: The Percentage Sample should be entered in the position of the Baud Rate which is selected from the range between 25% and 75%, and the default of the Baud Rate is 60%. The resolution can be adjusted to 1%.

Baud Rate: The Baud Rate can be set to Integer or selected from the pull-down menu (10000, 20000, 400000, 500000, 800000, 1250000, 2000000, 2500000, 4000000, 5000000, 6600000, 8000000 and 10000000) manually, and the default is 125000. If the Auto is selected, the Baud Rate can be calculated by the main program automatically and displayed on the CAN 2.0B dialog box.

Data Reverse Decoding: If it is selected, the data can be decoded in reverse.

After End Packet happens, just begin to analyze: If it is selected, the signal will be decoded when the End Packet appears.

When CAN Data for expansion, combine Basic ID and ID: If the option is selected, the Basic ID and ID will be combined.

The Del is displayed in CRC Field: If it is selected, the Del will be displayed in the CRC Field.

Protocol Analyzer Color:

The protocol analyzer colors can be varied by users.



Operating Instructions

Open the user interface of the Logic Analyzer.

			(%01) (%/%000000-0000	0+(LaberS)				ARK.
the Buttional To			and the second se			and the second second	-	alfin
0498		And a state of the second s	28 28	states where it is not the state of the stat	the second se	N . Page Page	and a constant of the second se	-
Gamier 100ms		Dreeday i	Pasters	25 L Ls 14		Pleaght 26	Trigger Detry A - B = 3us	Pfbex-
Tutar 20 K Bus			Marge-25us -3.0vit	8 Pois 1 Suo -		+ 1.5us +	Comps-Illate No.	
Bue/Signal	Tigps	The	- nuesenne	the contract of	506e	1.00W01010660	(Tag. 34.)	254
# AD IN	CHL.	-						
🖉 A1 (1)	10000000	0.805						
# 42 M	1.112							
43 11	12000							
2 44 54	1.00	00						
	目的の	1.05						
# AL N	1.00							
1000	1388.33	- 36						
# 80 10	304	00						
# 81 11	- 52	1 90	1					
₹ 82 .40	00	00						
. 87.01	1.88.7	- 100						
2 24 24	186	1000						
₹ 85 In	1381	1981						
# 85. 10	.82	102						
# 82 32	1238.23	1.882						
* co ==	143	108						
# CI ()	1280							
∉ α α	34	185						
	1200	1.000						
C+ 11	13011	100.						
		• •	1		1			
Facty							8140	0010

Fig4-128 - User Interface

Sample the CAN 2.0B signal or open the sampled waveform.

25 10 20 10 10 10 10 10 10 10 10 10 10 10 10 10		Desplay Put 1		40 +1 + Plaught 26 +	Count 1 Trugger Detay 5in A - 8 = 16 182426as Compar-Hale 255.683
Invitional	Titagen			4.233564 100 498724 511 5228754 047 4167374	
# AD 10	X.	0.	16.775ma		150 299ms
	100	0		167 690ms	
# 42 M	1.82	0		167.696ms	
AL-11	130670	0.0		167.695ms	
# At 14	1.00	10		167.695ms	
# 85 -41	12.56.0	0.0		167.695ms	
ALM:	- 20	a		t67.695ms	
100	1.38.1	- 40.1		167.695ms	
* 10 11	104	100	t6.775ma		150.288ms
# # 11	- 52.1	- 48		167.695mi	
¥ 82.42	00	(0)		167.695ma	
. 87.01	- 88.7	100		167.695ms	
# 84 34	36	0		167.695ms	
# 85 IN	1381	28		167.695ms	
¥ 86.10	.82	(0)		167.695ms	
# 12 X	1281	0		167.595ms	
* 00 CE	100	(0)		167.695ma	
# G ()	1280	0		167.695ms	
∉ α :::	34	(1)		167.695ms	
	12788	A CONTRACT OF		167.63dms	

Fig4-129 - CAN 2.0B Waveform



Group the signal channels into Bus.

	Pi		1 P PP	128K - 44	200MHz =	10%	• to + Page	T Court 1 -
1 55 k h	0.0			22 2 L L	L M 1+ +1			Trigger Detay Sea
74.776833us 187.60578ms			Page 138.649912us Range 1.729360mil	 APost87.81 B Post104.0 			17.851299us	A-8+18182424us * Compe-Rate 255383
Invitional	Trigge	The						
1 AD 10	X.		CHARLE INCOMENT.	16.775ms	COMPLEX CONTRACTOR	states and the second second	Constant per terro with the	1201293pe 1420192pe 1409
	amplifing Distila						67 695ms	
AL AL CO	haven Seta						67 695ms	
	nako walet		24				17.695ms	
	our Lead-						67.695ms	
	everse.							
	rospierto Bui		0/46		_		n7 mildeni	
	234 Parts		CHANNE				67 695ma	
	At Chavel	-					67.695ms	
- DU - 200	igo Ourvel elete Ourvel	V.		16.775ms				150.288ms
	elete Al Char					1	67.695ms	
1 R E 8	ectore Defad	t Charren				1	67.695mi	
10 11 F	amat Rose					1	67.695ma	
A 11	mane	_				1	67.695ms	
· 15 11	17.88 11	1.00				- 8	67 695ms	
A 10	56	19				- 1	67.695ma	
1 87 10	1.82	-10				1	67.695ms	
# C0 CII	30	0				1	andrea Ta	
C (1)	1.201	- 10	-				67.695ms	
a	12	0					67.695ma	
0 11	1.20	-					67.695ma	
	-	-					67.695ms	

Fig4-130 - Group into Bus

Select the Bus Property to set up the Bus Property dialog box .

2 9 0 4 1 1 15 4 1 1 17 10575ma	00	Complay P	1 5 128K		Cover 1 Trigger Delay Gas A-8 = 18.183444 Comps-Rate 295.880
Bur/Signal	Tigge	The .		234 222254 3 4 4 4 1 2 4 5 1 3 5 221 5 4 1 5 1 2	
Bet				UKI TITTI T THE OKI	
Sampling 5			16.775ms		150 298ms
· In Distance				167 695ms	
Anutog Wa			1	167.695ms	
Renter .				167.005ms	
				167.695ms	
. lingnach		Orieli		167 695mp	
All Curr	wi.i.			167 £95ms	
				167.695ms	
· Delete Al			16.775ms		150 288ms
	Ind Charle	÷		167.695mp	
e Format Ro	-	,		167 £95ms	
Batate	-		1	167.695ms	
# H IV.	1.99.2	- 48		167.695ms	
# 85 H	00	10		167.695ms	
# M TE	1.88	- 40		167.695ms	
001	128615	0		167.695ma	
# 05 ,08	1288.21	一些		167.695ms	
< G 11	19413	0		167.695ma	
				167 695ms	

Fig4-131 - Bus Property



Select the decoding function of the protocol analyzer CAN 2.0B and select OK to confirm.

2 1 2 2 4 1	A Property of Street, of	- 74.7 Desplay P	b bb 128K → 40 250Mete • 100K → 66 ↔ 200g 1 6433 ↔ X 26 5 5 6 • 5 Height 26 26 • 130 64902246 A 7 8 5 1202046 • 6 7 8 7201000 • 7 6 • 0 • 125 Height 26 • • 0 • 0 • 125 Height 26 • • 0 • 125 Height 26 • • 0 • 0 • 125 Height 26 • • 0 • 125 Height 26 • • •	Count Trigger Delay Set A - 0 + 16.11D104es Comps-Rate 255.800
Inv/Signal	Trippe	Titue .	* WINNESS	1,20129900 (1,82019700) 2,008
Batt		0 .	ha Proverty 8	
#A0 ==	x	0	Bus Setting	150 298ms
# A1 /1	1000	0	City College	
C A2 41	1.007	-0.1	T knobier (k) (respective)	
A2 /11	00	0	Fingthe	
* 24 Sec.	1.38.0	1.001	Produced Analysis Setting	
# AS	26	700	F Pratecol Analyses Parameters Config	
144	1.38	- 48-	C 20000LG LA LAVIRE MODALE VI.11.00(CN01)	
6 D 10 .	00	100	 DISPOSITING A RECORDED VIOLATING (2010) TEROPLICIA PEOP PODALE VIOLATING (2010) 	
# 10 H	62.1	- 48	/* ZEROPUS LA 12C MODULE VE.03.81(CN01)	150.288ms
* 11 H	00	(19)	P. 20ROPLUS LA LED Pitch Array MODILE, VI. 00.00(0001) P. 20ROPLUS LA SPEMODULE VI. 13.03(0001)	
# 82.10	1.00	- 48	P. 25R PULIS LA GART PRODULE V2.14.00(OND1)	
ED 111	20	0		
# 84 St.	1.88.7	100	G Law the Dole Pert	
* #5 11	82 -	0	Non-Personal Academy	
# M II	1238	-	Cont Cent I Heb I	
101	00	0		
e ce : ca	1.381	-00-	167.695ms	
< C1.10	194	(0)	167.695ms	
a a	1.200	1.00	167.695ms	
00	126	1/ 63	167.095ms	

Fig4-132 - CAN 2.0B Bus Property Setup

Double click the ZEROPLUS LA CAN 2.0B MODULE V1.32.00 (CN01) to set the Protocol Analyzer CAN 2.0B dialog box.

PROTOCOL ANALYZER CAN 2.0B	x
Configuration Packet Data Format Register	
Pin Assignment	Start Packet Format
Protocol Analyzer Name: Bus1	I11Bit Start
Channel: 🗛	C 0 Bit Start
Protocol Analyzer Property	
Percentage Sample: 60%	Data Reverse Decoding After End Packet happens, just begin to analyze When CAN Data for expansion, combine Basic ID and ID The Del is displayd in the CRC Field
Protocol Analyzer Color Start Control CRC	Error ACK
End ID Data	Overload NACK
ОК	Cancel Default Help

Fig4-133 - Protocol Analyzer CAN 2.0B Setup



Click OK in the Protocol Analyzer CAN 2.0B dialog box to complete the CAN 2.0B Setting.

	00	Carried State of Lot of	2 ► 3 = 128K = 30 = 2280MHz = = 10% = 4 ← Page 1 = Count 1 = 68729 = ≤ 1 = 228 ↓ 2 ± ■ 0 = 21 ← Height 26 = Tagger Delay Sim
# 10.488729vs c167.69579ms			n 255.78/1974a A Pais 37.551.298vic • A - T + 87.851.298vic • A - 8 + 16.102434vic • B - 75.8270174i • B - 16.102434vic • Comp. Rate 255.883
Bur/Signal	Tippe.	The .	25.494626.m 79.29626.50.101.102913.m 103.44255.4m 225.79(115/m 288.13494.m 240.495482.m 282.822125.m 445.165768.m 49/ 503
Bart (CANED IN		0.1	
#A6 ==	×	0	40 01500 40 01500 40 00500 40 0100 40 01500 40 0100 40 03500 18 16 16
CAL NI		0	167.695ms
1 K 41		100	167.695ms
A2 41		10	167.005ms
* 24 -2+	1.20	01	167.895ms
✓ AS	100	0	167.695ma
1 Al. C.		- 40.	167.696ms
6 D N.	101	100	167.696m
· 10 10	50	- 48	40.01xg 40.015xg 40.025xg 40.015xg 40.01xg 40.015xg 840.02v1 8 8 16 16 24
# 85 (H)		(49)	167.695ms
ef 82.10		10.1	167 696ms
- 83 111	35	0	167.696ma
# 84 14	1381	10.	167.695ms
* 8 =	32	(0)	167.695mi
* M II	1381	0	167.695ms
000	143	0	167.695ma
• ca :::	120	0	167.695ms
* 0.0	32	0	167.695ms
-q -	120	100	167.605ma
	in the same in some	And in case of the local division of the loc	167.695ms

Fig4-134 - CAN 2.0B Decoding



4.5.7.2 Protocol Analyzer CAN 2.0B Packet Analysis

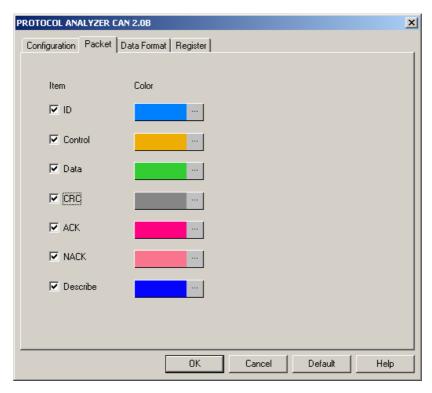


Fig4-135 - Protocol Analyzer CAN 2.0B Packet dialog box

Packet color can be varied by users.

The Packet displays with the waveform as below:

Nor-Signed Team	NOTES
••• × 0 16.775ms 40.0150g 40.0150g 40.0050g 40.010g 40.010g 40.010g 40.010g 40.010g 40.010g 40.010g 40.010g 40.010g 40.0150g 40.0050g 40.0150g 40.	the second s
All All Bit	40.0104 [40.01504] 4
All Bit Bit <td></td>	
All All Bit Bit <td></td>	
At St St<	
AS SS SS<	
Ab 32 48 167.555ms AD 50 167.695ms 167.695ms AD 16.775ms 140.015dg 40.015dg AD 16.775ms 140.015dg 40.015dg AD 16.7695ms 167.695ms	
10 16<	
★1 H 10 167.055m	
	40.015up 40.01un 4
√ 82 1 . 167.695ms	
🚅 83 HI 38 00 167.695ms	
# 84 64 167 695ms	
✓ # = 0 0 167.695ms	
Setting Antenh Expert SechTaranter	
Packet # Name Treastern: Ball 22 Still BE St. RTH RELINCE Data (DC) 200	

Fig4-136 - CAN 2.0B Packet List Displayed with the Waveform



4.6 Compression

The compression function enables the system to compress the received signal and has more data stored in per channel.

4.6.1 Software Basic Setup of Compression

Step1. Set up RAM Size, Frequency, Trigger Level and Trigger Position as described in Section 4.1.

- Step2. Set up the trigger edge on the signal or the Bus to be triggered.
- Step3. Click 🔟 icon, or click the compression function from the Sampling Setup dialog box then click Apply and OK to run.

	Sampling Setup	×
	Clock Source Asynchronous Clock Trequency: 10MHz	
 File Bus/Signal Trigger Run/Stop Data 	Synchronous Clock C External Clock Rising Edge Frequency: 100KHz Falling Edge (Min:0.001Hz, Max:100MHz) Note: The external clock voltage level is the same as the port A trigger level	
Image: Channels Setup Scale: Total:: Group into Bus Ctrl+G Ungroup from Bus Ctrl+U Expand Collapse	Sampling RAM Size RAM Size: 2K Compression Mode Signal Filter Signal Filter Setup Signal Filter Setup	
Format Row Rename	Apply OK Cancel Restore Defaults Help	

Fig 4-137 – Compression Mode

Step4. Click **Run**, and then activate the signal from the tested circuit to acquire the result on the waveform display area. Fig 4-138 shows the result before and after compression has been applied.

de Him	<u> 1 0 2 1</u>	• 10 Binglar Binglar	Fea Una A Pus -150as + A	Height 30 - - T = 190es + - T = 150es -	Count 1
Pes/ligial	Dige	Filter			
🗸 AG	100.0	31.	Unknown		
✓ A1 32	1.85.13	. 25	Unknown		*****
# A2 10	2.30.2		Unknown		
A3:47	22		Unknown		
# A4 .11	0.56		Unknoen		
45 45	28.73	. 35	Unknown		
* AL	0.500	32	Unknown		
W 42.11	20	20	Unknown		
e 80 mm	1-35111	X	Unknoen		
e 81 11	1.521	1	Unknom		
# RI =	128023	- 22	Unknown		
. 10 11	1 22	20	Unknom		
	1.35	20	Unknom		
et 15	1-321-3	1	Uriknom		
· N 11	1150.11	-	Unknown		
# M 11	1.26	20	Unknown		



1 105 23m	<u>19</u>	- 10nn Binglag Fea Binglag San		- Height 30 • A - T = 150m • B - T = 150m •	Compr-Sala 10.021
bulligial	Diger	1221a	-12000 - +++++++++++++++++++++++++++++++++		rthus
🗸 AG	30.0	0.	Unknow		
✓ A1 32	185.73	- 57 -	Unichow	a.	
# A2 10	0.50.2	12	Unitnos	n	
A3.47	52	2	Unitnost	n	
# A4 .11	0.56	10	Unitnos	n.	
4 45 44	28.1	- 10-	Unknow	n	
* AL	0.500	-	Urstnow	n	
d 42.11	50	- 0	Unknow	n	
e 80 mm	1-36	0	Unknow	n.,	
e 81 11	521		Unknow		
# NL =	1 50 7 3	- 83	Unknow	n	
. 10 11	20	-	Unknow	n:	
	1.36	0	Unknow	n.,	
* 65 15	521		Unknow	n	
* N 11	1 50 1	8	Unknow	n	
400	20	10	Unknow	n	
/ 0 0	- 38.1	-	Unknost		-

Fig 4-138 – Before and After Compression

Using 2K memory depth, before Compression has been applied, the total of the data was 20.48us; after the Compression had been applied, the total of the data was 205.23us, therefore, the compression rate is 10.021.

Tip: Click 📓 icon to view all data, and then select the waveform analysis tools to analyze the waveforms.

Step5. Click the compression icon again or click off the compression function to stop compression.

Tip: Compression cannot be applied with the signal filter function at the same time.



4.7 Signal Filter and Filter Delay

The function of the Signal Filter and Filter Delay allow the system to keep the required waveform, and filter out the waveforms that aren't required.

4.7.1 Basic Setup of Signal Filter and Filter Delay

Software Basic Setup of Signal Filter and Filter Delay

- Step1. Set up RAM Size, Frequency, Trigger Level and Trigger Position as described in Section 4.1.
- Step2. Set up the trigger edge on the signal or the Bus to be triggered.
- **Step3.** Click icon, or click the Signal Filter Setup button on the Sampling Setup dialog box or select the item form the pull-down menu of the Bus/Signal and then the Signal Filter Setup dialog box will appear.

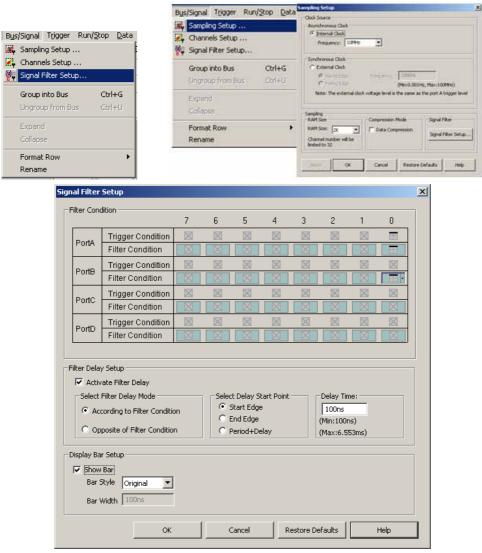


Fig 4-139 – Signal Filter Setup

Set the high level as Filter Condition on the signal A1.

Step4. Signal Filter Setup

- 1. Setup the Filter Condition as or unterstanding on the signal to be analyzed.
- 2. Click OK, then click Run to activate the signal from the tested circuit to the Logic Analyzer.
- 3. The system will display only the waveforms of the signals which are qualified by the Filter Condition.

Bus/Signal	Trigger	Filter	-20 -15 -10	-5	5 10	15 20
🖌 🗛 🔪	Z		311. 795us	15.88	30. 525us	20. 4us
🖌 AI AI			309. 055us			
∉ A2 A2					655.36us	
✓ A3 A3					655.36us	
# A4 A4					655.36us	
🖌 AS AS					655.36us	
🥑 A6 A6	20				655.36us	

Bus/Signal	Trigger	Fiter	
e ad A0	Z		# 18.27us
🖌 A1 A1		· •	x 388. 33us
			8 388. 33us
🥑 A3 A3			¥ 388. 33us
44 A4			¥ 388. 33us
« AS AS			¥
🥑 AG AG			#

Fig 4-140 – Without/With Signal Filter Setup

The first picture shows the result without any signal filter setup.

The second picture shows the result which has set the high level on the Filter Condition of the signal A1. Only the waveform with the high status of A1 is displayed.

Step5. Filter Delay Setup

- 1. Click on the Activate Filter Delay as shown in Fig 4-141.
- 2. Click on the According to Filter Condition or the Opposite of Filter Condition to select the waveforms to be kept.
- 3. Click on the Start Edge, End Edge or Period + Delay to set the Start Point of Filter Delay.
- 4. Type the value of the Delay Time into the column of the Delay Time.
- 5. Click OK, then click Run to activate the signal from the tested circuit to the Logic Analyzer.
- 6. The result will be displayed in the waveform display area as shown in Fig 4-140.
- Step6. Stop Signal Filter/ Filter Delay

Click **Stop**, then click **Signal Filter Setup** and select **Cancel** from the Signal Filter Setup dialog box to stop the Signal Filter or the Filter Delay Setup.

- Tip: Click Stop to check the conditions of the Signal Filter or the Filter Delay Setup, if there aren't any results.
- Tip: Click icon to view all the data, and then select the waveform analysis tools to analyze the waveforms.

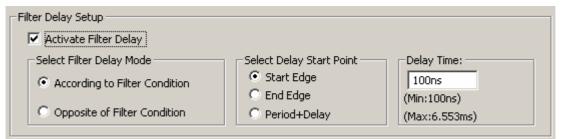
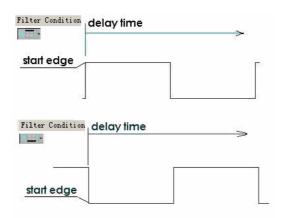


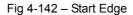
Fig 4-141 - Filter Delay Setup

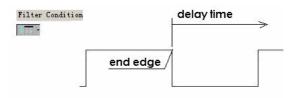
Tip: Definitions of the Start Edge and the End Edge and the Period + Delay are listed as Figs 4-142, 4-143,

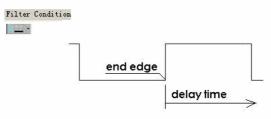


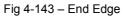
4-144 and 4-145.

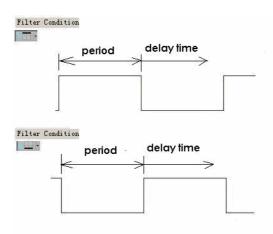














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1, IS	Tringer	7	6	5	4	3	2	1	0 7
PortA	Trigger Condition Filter Condition								
	Trigger Condition						X	X	
PortB	Filter Condition								
PortC	Trigger Condition	\square	\boxtimes	\boxtimes	\square	\boxtimes	\boxtimes	\boxtimes	\boxtimes
FUILO	Filter Condition						X		X
PortD	Trigger Condition Filter Condition							X	\otimes
Select	y Setup vate Filter Delay Filter Delay Mode cording to Filter Conditi posite of Filter Conditic		С в	t Delay S Start Edge End Edge Period+De			Delay Tim 1s (Min:100n (Max:6.55	s)	

Fig 4-145– Filter Delay Setup

The delay time of signal A0 is 1 us, which is the condition of the Filter Delay Setup.

Step 7. Signal Filter Time Interval

1. Click Show Bar to know the length of the tested and deleted signal as shown in Fig4-146 below.

Display Bar Setu	q.						
🔽 Show Bar							
Bar Style	Original	•					
Bar Width	100ns						
		ОК	Cancel	Restore	Defaults	Help	1

Fig4-146 - Display Bar Setup

2. The bar has two styles, which are Original and Bar; the default is Original style, which denotes the bar function cannot be used. When selecting Bar style, the bar function can be activated.

- 3. Bar Width, when Bar style is selected, the bar width can be set by users.
- **Tip:** The minimum bar width is 1; the maximum bar width is 65535. If the value exceeds the range, or the font is not according to the requirement, a tip window will appear.

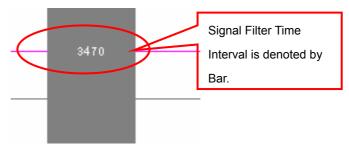


Fig4-147 - Signal Filter Time Interval



Tip: The Signal Filter Time Interval is limited under the following situations.

A: The Filter Delay and Display Bar of Signal Filter are not available under the compression mode.

B: The Filter Delay and Display Bar of Signal Filter are not available under the double mode.

C: The final two data are NULL.

D: Logic Analyzer supports the Signal Filter Time Interval function on condition that the time interval between signal filter must be more than two clocks.



4.8 Noise Filter

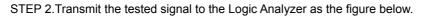
The Noise Filter function enables the system to filter the waveform that doesn't meet users' requirements.

4.8.1 Basic Software Setup of Noise Filter

STEP1. Click **Data** on the Menu Bar, then select 2 Noise Filter to activate the noise filter function as the figure below.

<u>D</u> ata <u>T</u> ools <u>W</u> indow <u>H</u> elp		
Select an Analytic Range		Noise Filter
🤠 Noise Filter		
🔯 Bus Width Filter		Noise Filter: None
Data Contrast		Noise Filter: None
👪 Find Data Value	Ctrl+F	Cancel
📮 Find Pulse Width		

Fig4-148 - Noise Filter



Bus/Signal	Trigger	Filter	۲	1 1		- <u></u>		4	-	4		pro	1	10	a	1	1	-5	p. 18	. 74			١,	1		60
🖌 AO AO		- 12	1	1 1	1 1	ι 1	1 1	1	1	1	1 1	. 1	1	1	1	1	1	1	1	2	1	1	1	1	1	1
🝼 A1 A1			2	2	2	2		2	2		2		2	2	Ī	2	1	2	1	2				2		2
∉ A2 A2				4		4	1		4	1		4			4			3			4				4	
🥑 A3 A3					8		1			8	3			Γ		7							8			

Fig4-149 - Tested Signal

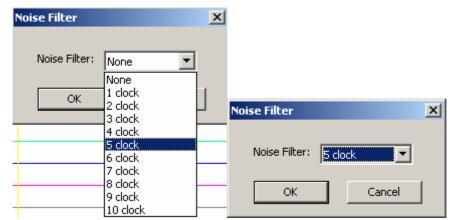


Fig4-150 - The condition of Noise Filter is 5clock.

STEP 4. After filtering, the waveforms that are not bigger than 5 clocks are deleted.

Bus/Signal	Trigger	Elter		 	10 -5	 	5 10	15 20
e da 🍡	- 12	- 12				20	48	
AI AI						20	40	
₹ A2 A2	121					20	48	
🥣 A3 A3			8	8	7	8	8	8

Fig4-151 - Waveforms after Filtering

STEP 5. Reserve the original waveform: open the Noise Filter window, and then select None, the waveform will be restored.

Noise Filter		×
Noise Filter:	None	
	None	
ОК	1 clock	
	2 clock	
	3 clock	
	4 clock	
	5 clock	
	6 clock	
	7 clock	
	8 clock	
	9 clock	
	10 clock	

Fig4-152 - Restore the Waveform



4.9 Data Contrast

In order to make users analyze the Data and contrast the difference of Data easily, there are adding the function of Data Contrast. The function of Data Contrast is used to compare the difference of two signal files of the same type. One is the Basic File and the other is the Contrast File. It can line out the different waveform segments of the basic file in the contrast file. Meanwhile, it can count the number of the difference.

4.9.1 Basic Software Setup of Data Contrast

STEP 1.Click **Data** on the Menu Bar, then select X to open the Data Contrast Settings dialog box.

	Data Contrast Settings	<u>위 치</u>
	Activate Data Contrast Contrast Files LaDoc1 Contrast File: LaDoc2 Contrast Beginning Point Ds D D D None	Files Display Mode Display Mode Display files horizontal Roll the contrast waveforms synchronization Display files the contrast differences Apply
Data Tools Window Help	Contrast: Ratistics	Provious Next Close
🔁 Select an Analytic Range	Contrast Result	Error Stat.
noise Filter	A0(A0) FAIL	6226
	A1[A1]	24916
🔯 Bus Width Filter	A3[A3] FAIL	1
👤 Data Contrast	A4[A4]	2
	A6[A6] FAIL	2
TT et le la la la calaci	A7[A7]	2
👪 Find Data Value Ctrl+F	BI[B1] FAIL	2
💻 Find Pulse Width	[82[82] FAIL	2

Fig4-153 - Data Contrast Interface

Activate Data Contrast: Click the checkbox to activate the function of Data Contrast.

Basic File: It is the standard contrast file.

Contrast File: It is used to compare with the Basic File.

Contrast Beginning Point: Select the point to begin the contrast, based on the basic file.

Contrast End Point: Select the point to end the contrast, based on the basic file.

Error Tolerance: It is the allowable time error when setting data contrast.

Display files horizontal: Display the two files horizontally to see the contrast more clear. It is not selected by default.

Roll the contrast waveforms synchronization: Roll the two horizontal files synchronously. It can be selected after **Display files horizontal** is selected.

Pin Assignment: Users can select the contrastive channel.

Perform Contrast: It can activate the Contrast at once.

Contrast Result: It displays the same contrasted result and the different contrasted result with PASS and FAIL respectively.

Error Stat. : It displays the number of discrepant parts.

Tip: For this function, Data Contrast, we provide the SDK Development Tool for users. Users can customize the Data Contrast Interface according to their requirements. We has packed the Data Contrast UI as the GUI.DLL and designed an interface which is used for the communication between the GUI.DLL and Main



Program. The GUI adopts the Non-modal Interface design, which can make the GUI Interface and Main Program Interface switch freely. When users activate the Data Contrast function, the software will search whether there is a GUI. DLL or not, then it can judge whether there is a user-defined Interface. If there is a user-defined Interface, the GUI.DLL will take effect; if there isn't, the embedded Data Contrast Interface will be activated.

STEP 2. Display the contrast results in the Data Contrast dialog box.

Tip: After pressing Perform Contrast, it will display the contrast information in the contrast result. The below contents of the box are the contrast information. The information is relative simpleness; if users don't want to understand more details, you can know whether the signals of the two contrast files are completely the same or not.

ta Contrast Settings 7 Activate Data Contrast		?
Contrast Files	Files Display Mode	
Basic File: LaDoc1	Display files horiz	rontal
Contrast File: LaDoc2	Roll the contrast	waveforms
	synchronization	
Contrast Beginning Point Contrast End F	Point Error Tolerance IV Display files the	contrast differences
Ds Dp	None Apply	
<< Hide Result Pin Assignment Pi	erform Contrast Provious Next	Close
	erform Contrast Provious Next	Close
<< Hide Result Pin Assignment Pin Assignment	erform Contrast Provious Next	Close
	erform Contrast Provious Next	Close
Contrast Statistics		Close
Contrast Result A0(A0)	Error Stat.	Gose
ontrast Statistics Contrast Result 40(40)	Error Stat. 6226	Gose
Contrast Statistics	Error Stat. 6226 24916	Close
Contrast Relistics	Error Stat. 6226 24916 14 1	Close
contrast Statistics Contrast Result A0(A0) A1(A1) A2(A2) FAIL A2(A2) FAIL A3(A3) FAIL	Error Stat. 6226 24916 14	Close
Contrast Statistics Contrast Result A1[A1] FAIL A2[A2] FAIL A3[A3] FAIL A4[A1] FAIL A5[A3] FAIL A4[A4] FAIL	Error Stat. 6226 24916 14 1 2 2	Close
ontrast Statistics Contrast Result A0(A0) A1[A1] A1[A1] A2[A2] FAIL A2[A2] FAIL A2[A2] FAIL A2[A2] FAIL A2[A2] FAIL A2[A2] FAIL A4[A4] FAIL A4[A4] FAIL A4[A4] FAIL	Error Stat. 6-226 24916 14 1 2	Close
contrast Statistics Contrast Result Q(A0) FAIL AQ(A0) FAIL AQ(A2) FAIL AQ(A2) FAIL AQ(A2) FAIL AQ(A2) FAIL AQ(A2) FAIL AQ(A2) FAIL AQ(A3) FAIL AQ(A4) FAIL AQ(A2) FAIL	Error Stat. 6226 24916 14 1 2 2 2	Close
ontrast Statistics	Error Stat. 6-226 24916 14 1 2 2 2 2 2 2 2	Close

Fig4-154 - Display the Contrast Results in the Data Contrast Settings Dialog Box

A0[A0].....FAIL: It indicates that there are differences in the channels of the two files.

B0[B0].....PASS: It indicates that there is no difference in the channels of the two files.

STEP 3. Display the contrast results in the waveform windows. See the figure below.

Tip: It contrasts the two data files in the waveform area. The contrast waveform and the basic waveform are displayed horizontally; we can roll the mouse to contrast the waveform files; the difference of the waveforms will be lined out with the red wave line "-------" in the contrast files.



🐝 ZEROPLUS-LAP-C (321	000) Stani	lard V3.1	12 (CR01) (S/H:000000-0000) - LaBac2	
			[ools Window Kelp	
1			10 ► ► ► 512K • ## ## 50MHz • ## 50% • ## # Page 1 • Count 1 •	
	(7 🖬) 🖻	2.68		Font
LaDoc2 Scale:2.682784ms Total:10.48576ms			Pos:=5.24286es A Pos:140.000111ns ▼ A = T = 140.000111ns ▼ A = B = 140.000408ns ▼ Range:=5.24286es ~ 5 B Pos:=0.000297ns ▼ B = T = 0.000297ns ▼ Compr=Rate:No	×
Bus/Signal	Trigger	Filter	-50.03054as -45.40462as -32.0707as -10.65670as -5.2420-5 0.17106as 21.50430as 04.9903as 40.41202as 61.0267	4
▼ Bus1 (SPI)	•			1
●A0 A0				-
A1 A1				~
6 A2 A2	N			~
EA EA 🏷				~
₹ A4 A4				~
✓ A5 A5				2
🐔 LaDoci				l ×
Scale:670.696us Total:167.674075es			Pos:=16.77510ex A Pos:=16.77014ex A = T = 16.77014ex A = T = 16.77014ex A = B = 150nx A = 150nx A = 150nx	
Bus/Signal	Trigger	Filter	-30, 1891ms -26, 85562ms -23, 48214ms -20, 12866ms -14 518ms -13, 4217ms -10, 06822ms -6, 71474ms -3, 96126ms - 🕂 790	-
Bus1 (HDQ)	·	⊗ •	Unknow	Ц
•AD AD	N	8	16.775ms	
•A1 A1		8	167.674ma	
●A2 A2		0	167.674ms	
🧭 🗛 🔪		8	167.674ms	
🥑 🗛 🗛		\otimes		
AS AS	R F	- - -		3
Ready			Endi 1990	

Fig4-155 - Display the Contrast Results in the Waveform Windows

Tip:

The Data Contrast function is available for the LAP-321000U-A , LAP-322000U-A, LAP-C(162000), LAP-C(321000) and LAP-C(322000) Modules, and it is not available for the LAP-16032U, LAP-16064U, LAP-16128U, LAP-32128U-A , LAP-C(16032), LAP-C(16064), LAP-C(16128) and LAP-C(32128) Modules.



4.10 Refresh Protocol Analyzer

The Refresh Protocol Analyzer function enables the system to analyze the data between Ds and Dp again.

4.10.1 Basic Software Setup of Refresh Protocol Analyzer

STEP 1.Click **Tools** on the Menu Bar, then select 😟 or click 💁 on the Tool Bar directly to refresh Protocol

Analyzer.

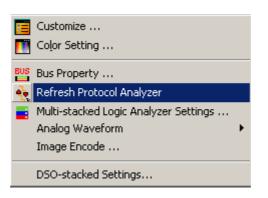


Fig4-156 - Refresh Protocol Analyzer

STEP 2. Transmit the tested Protocol Analyzer signal to the Logic Analyzer, for example Protocol Analyzer SPI.

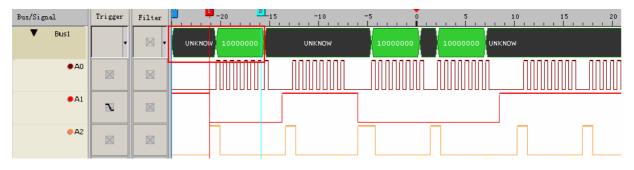


Fig4-157 - Waveform before Refreshing

STEP 3. Choose Select an Analytic Range to select the analysis range, and drag Ds Bar to B Bar.

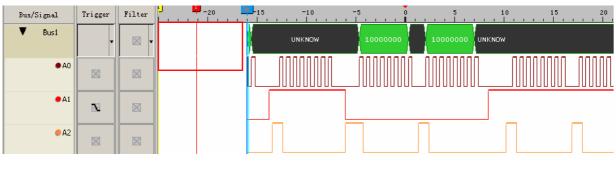


Fig4-158 - Drag Ds Bar to B Bar

STEP 4. Click , the Logic Analyzer will analyze the data between Ds and Dp.



Bus/Signal	Trigger	Filter	-20 -	L ₁₅	-10	-5		5	10	15	20
▼ Bus1	•		ı	NKNO	N	1000	0000	10000000	UNKNOW		
• A0											
• A1	N										
● A2											

Fig4-159 - Analyze the Data Between Ds and Dp

S	TEP 5.Click	🚢 a	gain, th	e wavef	orm return	the original state				
	Bus/Signal	Trigger	Filter		-20 ⁴	15 -10	-5 0	5	10	15 20
	▼ Bus1	T		UNKNOW	10000000	UNKNOW	10000000	10000000	UNKNOW	
	• A0									
	• A1	N								
	● A2									

Fig4-160 - Restore the Original State

Tip: The Refresh Protocol Analyzer function can come into effect, while the Ds and Dp are activated.



4.11 Memory Analyzer

Memory Analyzer enables the system to divide the packet format in the Protocol Analyzer and display the Address and Data in an independent list. It is better for understanding the relative relationship and status of the Address and Data in the operating process of the Protocol Analyzer. Users will know the operation when they use this function. It improves the efficiency of knowing the conditions.

4.11.1 Basic Software Setup of Memory Analyzer

STEP 1. Click **Tools** on the Menu Bar, then select 💻 to activate the Memory Analyzer function.

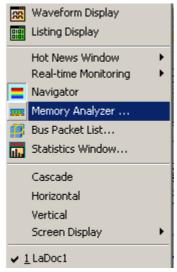


Fig4-161 - Memory Analyzer Interface

STEP 2. Open the Memory Analyzer dialog box

K	<< <	>	>> Opt	ion I	mport	Export	Merg	e R	efresh	Reset	Display Al	eration		#				
	Bus1(I2C)																	
Ī	Address	Write d	ata	Read data														
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
								Uni	used:0X00)~0X4F								
	0X50	0X00	0X79	0X89	OXAB	0XCD	OXEE											
						🗸 C	ompact Mod	de "Uni	used:0X60)~0X7F								
						C	omplete Mo	de										
						_												
																		•
	•																•	

Fig4-162 - Memory Analyzer Dialog Box

1. Compact Mode and Complete Mode:

Click the Right Key in the memory analyzer dialog box; there are two modes for selecting, which are the Compact Mode and the Complete Mode. See the two different figures:



(<< <	>	>> Op!	tion	Import	Export	Merge	R	efresh	Reset	Display Alt	eration		#				
	Bus1(I2C)																	
	Address	Write d	ata	Read data														1-
		0	1	2	3	4	5	6	7	8	9	A	В	C	D	E	F]
								Uni	used:0X0	00~0X4F								
	0X50	0X00	0X79	0X89	OXAB	OXCD	OXEE											
						🖌 🗸 Ca	ompact Mod	e <u>I</u> Uni	used:0X6	50~0X7F								J
						Co	omplete Moo	le 🛛										
						_												
																		_
	4																•	

Fig 4-163 - Compact Mode

×	<< < Bus1(I2C)	>	>> Opti	on	Import	Export	. Merge.		Refresh	Reset	Display Alte	eration		14				
		Write d	lata R	lead data	1													
	Address	Data	Address	Data	Address	Data	Address	Data	Addres	s Data	Address	Data	Address	Data	Address	Data	Address	
								_								.Unused:0)X00~0X4F	
	0X50	0X00	0X51	0X79	0X52	0X89	0X53		mpact Mode	NCD.	0X55	OXEF	0X56		0X57		0X58	
								🗸 Co	mplete Mod	le						.Unused:()X60~0X7F	
	_																	그
1	•																	

Fig 4-164 - Complete Mode

2. Buttons:

- : It is used to find the first packet.
- : It is used to find the previous packet.
- : It is used to find the next packet.
- >>>: It is used to find the last packet.

Option... : It is used to set the relative parameters for the List Window of the Memory Analyzer; see

the following Option dialog box:

Option			x
Bar Assignm	ent		
	Reaction Bar	A	•
Active Displa	ay Assignment —		
	Display Width	16	•
Color —			
Addr		Data(R)	
Data(W)		Alteration	
<u></u>	ОК	Cancel	Default



Reaction Bar: The default is the A Bar; the added Bar can be displayed and selected in the pull-down

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menu if users have added a new Bar. The data position of the Reaction Bar will be displayed in the List Window of the Memory Analyzer.

Note: The Ds/Dp Bar and T Bar can't be displayed in the pull-down menu.

Display Width: It is used to set the display width of the List Window of the Memory Analyzer; the default is 16. Users can select the 4, 8, 16 and 32 from the pull-down menu, and they also can input a value between 1 and 100.

Color: Users can vary the color of Addr, Data(R), Data(W) and Alteration as their requirements. The default color of the Addr is black; the default color of the Data(R) is blue; the default color of the Data(W) is red; and the default color of the Alteration is gray.

Import... and Export... The Export function

: The Export function can select the TXT or EXCEL format to store the

Data of the List Window of the Memory Analyzer; the Import function also can select the TXT or EXCEL formats to analyze the former export data.

Merge...

: It can merge with the different export files. See the Merge dialog box below.

1	2	3
Object file:	://10.txt	Open
File to merge:	2 <i>11</i> 11.txt	Open
		Cance

Fig4-165 – Merge Dialog Box

Object File:

1. It is the covered file, that is to say, it is a new file.

2. It can display the path of the "Object File" and the file name.

3. It can open the "Object File" by clicking the "Open" option.

File to merge:

- 1. It can create the new file with the object file.
- 2. It can display the path of the "File to merge" and the file name.
- 3. It can open the "File to merge" by clicking the "Open" option.

Refresh

: Pressing this button can refresh the data status of each Address data when there are

some alterations in the Bus Data

Reset : The data status of each Address will be cleaned out and returned to the original status by

pressing the button.

Display Alteration

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Exploy Accession is the Data in the List Window of the Memory Analyzer will be cleared by pressing this button and the List Window will display the alteration status of each cell. If the same Address has been written or read repetitively, the background of the cell will be gray and the list window will display the Data of the last packet. If the Address doesn't have any alteration, the Address Data will display the data of the Address without the background color. If it is the first time that the Address has been read, we confirm that the data of the packet has been altered.

: When users input the Address in this Edit Box and click the Find icon, it will go to the

corresponding position which is highlighted by the Blue frame.

STEP 3 .Display the Memory Analyzer function in the waveform window.

Tip: The Packet is read; the Address is 0X50; the Data are 0X00, 0X75, etc. in sequence.

x78.0034mii		Disatery Ro	arge 98.8147	1145	BPoi-	52.0004mi 52.0024mi		Ð-	T = 02.002	Hmi .+			D = Dui nur Ra	du:1013	63
Budgel	Tagger	(15+	49.610	104 <i>4</i> , 40.0	00057un /1	1.40172	17.402706	46.400023	6. 15.40	25ye , 101.4	11079-0	133 41 106	14	2,424234	111.63
Ball (12C)		10.1	a construction of the	1			0.50	0000	+ 0473	X 04	- X-	0623	- 64	45 X I	2057
•A0 =	x	10		52.29#	13							ШШ	ШШ		
- A1 - 11		0		52 2897	ns :	n	1 5	0.8us	96 8	25.418	3.6	9.4	9.6	R LI	94
# A3 40	(35)	10							78.603	Bress.					
AS .24	1.88.00	0							78 603	âmă					
* A4 33	(22.1	-30							78.603	îmi					
	. 58	0							78.603	imt					
# AL	-21	10							78.603	3mii					
ar 22 .22	. 56	100							78.600	imt					
★ 60 cm	-10-	- 49							78.603	3ms					
	• 1 •	• •	<u>l</u>			Jan.					C				_
cc < >) ketit2Q dahese <u>kerne te</u> D		ninpor	t Exper	1.5	1.0	Refresh	Baset	Dupley A	L A	1.8	- M	1	2 1	Ł	
0.50 0.50	(Caller)	Contract of the	ALC: NO.	C. Com	-4	rayand SXX	0-018	1	1	I	1	1	1	00000U	1
and the second second					t	Pused dist	0-007	0	11		<u>.</u>				·

Fig4-167 – Memory Analyzer Display



4.12 Multi-stacked Logic Analyzer Settings

The function of the Multi-stacked Logic Analyzer Settings is mainly for connecting the hardware of many Logic Analyzers which are the same type, and then use the software to stack the Logic Analyzers which are working independently. It can improve the functions of the Logic Analyzer, which are mainly manifested in two aspects, expanding the RAM Size and adding the number of the test channels.

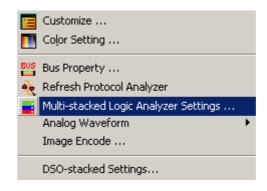
Tip:

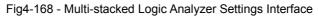
1. The max. number of the Multi-stacked Logic Analyzers is four. The RAM Size of the four Logic Analyzers can reach to 128K*4 and the test channels of the four Logic Analyzers can reach to 32*4.

2. The function of the Multi-stacked Logic Analyzer Settings is available for the LAP-32128U-A, LAP-321000U-A, LAP-322000U-A, LAP-C(32128), LAP-C(321000) and LAP-C(322000) Modules, and it is not available for the LAP-16032U, LAP-16064U, LAP-16128U, LAP-C(16032), LAP-C(16064), LAP-C(16128) and LAP-C(162000) Modules.

4.12.1 Basic Software Setup of Multi-stacked Logic Analyzer Settings

STEP 1.Click **Tools** on the Menu Bar, then select **I** to activate the function of Multi-stacked Logic Analyzer Settings.





STEP 2.Click 📕 to open Multi-stacked Logic Analyzer Settings dialog box.

Multi-stacked Logic Analyzer Settings	×
Activate Stack	
_ Stack Type	
Memory Stack	
C Channel Stack	
Please select the Logic Analyzer for stacking	
M1 S/N:000000-0000	
M2 S/N:000000-0000	
M3 S/N:000000-0000	
M4 S/N:000000-0000	
Synchronous Channel	_
A0	
C Synchronous Trigger Condition	
Rising Edge	
OK Cancel Help	



Fig4-169 - Multi-stacked Logic Analyzer Settings Dialog Box

Activate Stack: Click the checkbox to activate the function of the Multi-stacked Logic Analyzer; the default is non-activated.

Stack Type: Users can select the Memory Stack and Channel Stack; the default is the Channel Stack.

Please select the Logic Analyzer for stacking: It can display all the connected Logic Analyzers and the S/N code of them. The M1 indicates the first Logic Analyzer and the M2 indicates the second Logic Analyzer; M3 and M4 are similar to the previous. Users should select two or more Logic Analyzers, but the most analyzers users can select is four.

Synchronous Channel: Select the synchronous channel form the pull-down menu. The default synchronous channel is A0.

Synchronous Trigger Condition: Select the synchronous trigger condition. Users can select the Rising Edge, Falling Edge, High and Low from the pull-down menu. The default is the Rising Edge. The function of the Synchronous Trigger Condition can only be used in the Channel Stack, that is to say, it is disabled in the Memory Stack.

STEP 3. Display the function of Multi-stacked Logic Analyzer in the Memory Stack.

Tip: There are two Logic Analyzers to do the Memory Stack; the Synchronous Channel is A0; the data on the left of A Bar is captured by the first Logic Analyzer, the data on the right of A Bar is captured by the second Logic Analyzer.

		- 0.5	III ト ト ロ 128K - 祥祥 祥祥 200MHz · wu - 50% · 祥 中 Page 1 · Count 1 · S 5812272: · 王 光 記 記 記 記 記 記 記 記 記 記 1 · Count 1
e:10ns 1.81.92us			Positions A Positifications A - T = 150ns ▼ A - B = 300ns ▼ Range-250ns ~ 280ns B Positifications B - T = 150ns ▼ Compr-Rate:No
Bus/Signal	Trigger	Filter	62587.303 63447.552 64307.8 65368.049 66028.298 66838.547 67748.796 68609.045 69469.294 7
# AO (SYNC)	⊗ •	⊗ •	262144
# A1 A1	Z	0	1 490 490 489 490 489 491 460 516 978 980 981 980
	181	\otimes	262144
CA CA 🍤	20	0	262144
✓ A4 A4		0	262144
🝼 AS AS		\otimes	262144
🝼 A6 A6	120	0	262144
₫ A7 A7	25	8	262144
# 80 80	121	0	262144
# 81 81		8	262144
€ 82 82	121	0	262144
63 83		0	262144
6 84 84	8	0	262144

STEP 4. Display the function of Multi-stacked Logic Analyzer in the Channel Stack.

Tip: There are two Logic Analyzers for Channel Stack; the Synchronous Channel is A0; the Synchronous Trigger Condition is the Rising Edge; the former 32 channels (A0~A7, B0~B7, C0~C7, D0~D7) change into the 64 channels (A0~A7, B0~B7, C0~C7, D0~D7, E0~E7, F0~F7, H0~H7, I0~I7) channels.



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# A7 A7	122	8		120195	
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6 84 84	8	8		120195	
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4.13 DSO-stacked Settings

To use the DSO-stacked function between Logic Analyzer and DSO, it is necessary to install specialized software to connect if using the DSOs produced by other manufactures except our company.

If Tektronix oscilloscope is used for stacking, please download the <u>TEKVISA CONNECTIVITY SOFTWARE</u> V3.3.4 version or higher from the Tektronix Website.

If OWON oscilloscope is used for stacking, please download the Windows USB Driver from the OWON Website(http://www.owon.com.cn).

If PICO oscilloscope is used for stacking, please download the Windows USB Driver from the PicoScope Website(http://www.picotech.com).

If GwInstek oscilloscope is used for stacking, please download the Windows USB Driver from the GwInstek Website(www.gwinstek.com).

If Agilent oscilloscope is used for stacking, please download the Windows USB Driver from the Agilent Website(www.chem.agilent.com).

If BK Precision oscilloscope is used for stacking, please download the Windows USB Driver from the BK Precision Website(www.bkprecision.com).



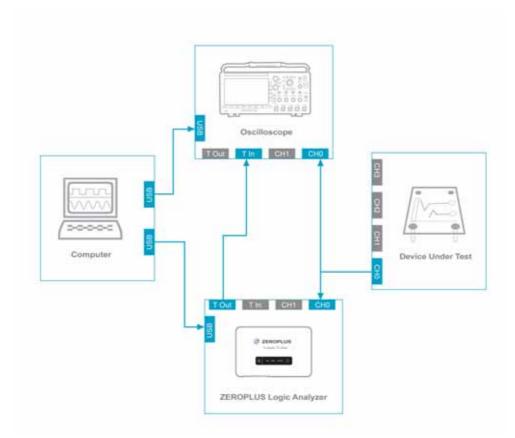
Supported DSO Models:

Oscilloscope Manufacturer	Models	On-line Mode			
	TDS1000 Series	USB			
	TDS2000 Series	USB			
Tektronix	TDS3000 Series	USB, TC/IP, GPIB			
	TDS5000 Series	GPIB			
	TDS6000 Series	In-built GPIB			
OWON	SDS7102 Model	USB			
PicoScope	3206B Series	USB			
GwInstek	GDS-1000A Series	USB			
Gwillster	GDS-3000 Series	USB			
Agilent	DSO5000 Series	USB			
BK Precision	2540B, 2542B, 2540B-GEN,	USB			
BITTEGSION	2542B-GEN	USD			

Operating Mode

(1) Host-Slave

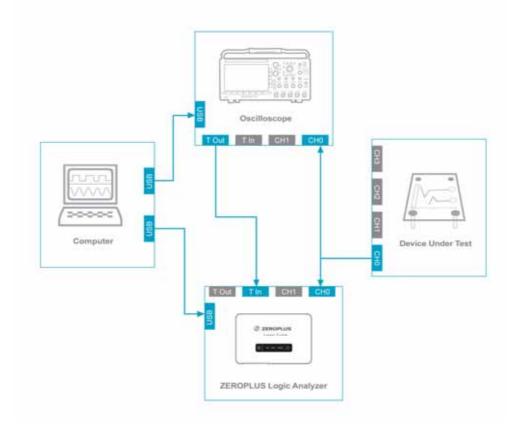
LA is the Host, DSO is the Slave. Connect the Trigger Out of LA with the Trigger In of DSO, when LA has been triggered, it will inform DSO to capture signal.





(2) Slave-Host

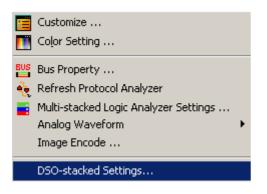
a) DSO is the Host, LA is the Slave. Connect the Trigger Out of DSO with the Trigger In of LA, and the LA uses external trigger. When DSO has been triggered, it will inform LA to capture signal.(LAP-B Series support)
b) DSO is the Host, LA is the Slave. Connect the Trigger Out of DSO with any channel of LA(users can define), which occupies one channel. When DSO has been triggered, it will inform LA to capture signal. (LAP-C series V3.10 higher version support)



Operating Instructions

STEP 1. Confirm the DSO is connected correctly.

STEP 2. Click the Tool on the Menu Bar, than select DSO-stacked Settings to open the dialogue box.





STEP 3. Set the Channel V/Div in the dialogue box.

DSO-stacked Sett	ings		×
Channel V/Div Setti	na		
DSO_CH1 V/Div:	2V/Div	DSO_CH2 V/Div:	2V/Div
DSO_CH3 V/Div:	2V/Div	DSO_CH4 V/Div:	2V/Div
Channel Setting			
Only display D	50		
DSO_CH1	DSO_CH2	🔽 DSO_CH3 🛛 🔽	DSO_CH4
			•••
Channel Height Set	ting		
DSO_CH1 Height:	80	DSO_CH2 Height:	80
DSO_CH3 Height:	80	DSO_CH4 Height:	80
Master			
Logic Analyzer		C dso	
DSO Settings	ОК	Cancel	lt Help

STEP 4. Set the Channel Waveform Color and select the DSO Channel to be displayed on LA software.

DSO-stacked Settings
Channel V/Div Setting DSO_CH1 V/Div: 2V/Div DSO_CH2 V/Div: 2V/Div DSO_CH3 V/Div: 2V/Div DSO_CH4 V/Div: 2V/Div
Channel Setting Only display DSO
Channel Height Setting
DSO_CH1 Height: 80 DSO_CH2 Height: 80
DSO_CH3 Height: 80 DSO_CH4 Height: 80
Master
• Logic Analyzer © DSO
DSO Settings OK Cancel Default Help



STEP 5. Select the Only display DSO according to users requirements.

DSO-stacked Settings
Channel V/Div Setting
DSO_CH1 V/Div: 2V/Div DSO_CH2 V/Div: 2V/Div
DSO_CH3 V/Div: 2V/Div DSO_CH4 V/Div: 2V/Div
Channel Setting
Only display DSO
I DSO_CH1 I DSO_CH2 I DSO_CH3 I DSO_CH4
Channel Height Setting
DSO_CH1 Height: 80 DSO_CH2 Height: 80
DSO_CH3 Height: 80 DSO_CH4 Height: 80
Master
Logic Analyzer O D50
DSO Settings OK Cancel Default Help

STEP 6. Set the Channel Height.

DSO-stacked Settings
Channel V/Div Setting
DSO_CH1 V/Div: 2V/Div DSO_CH2 V/Div: 2V/Div
DSO_CH3 V/Div: 2V/Div DSO_CH4 V/Div: 2V/Div
Channel Setting
Only display DSO
I DSO_CH1 I DSO_CH2 I DSO_CH3 I DSO_CH4
Channel Height Setting
DSO_CH1 Height: 80 DSO_CH2 Height: 80
DSO_CH3 Height: 80 DSO_CH4 Height: 80
Master
Logic Analyzer O D50
DSO Settings OK Cancel Default Help



STEP 7. Set the Master to be LA or Oscilloscope according to the hardware usage mode.

DSO-stacked Set	ings		×
Channel V/Div Setti	ng		
DSO_CH1 V/Div:	2V/Div	DSO_CH2 V/Div:	2V/Div
DSO_CH3 V/Div:	2V/Div	DSO_CH4 V/Div:	2V/Div
Channel Setting —			
🗌 🔲 Only display D	50		
DSO_CH1	DSO_CH2	🔽 DSO_CH3 🔽	DSO_CH4
····	•••		•••
Channel Height Set	ting		
DSO_CH1 Height:	80	DSO_CH2 Height:	80
DSO_CH3 Height:	80	DSO_CH4 Height:	80
-Master			
Logic Analyzer		C dso	
DSO Settings	ОК	Cancel	lt Help

STEP. 8 Press the DSO Settings button to open the dialogue box.

DSO-stacked Settings
Channel V/Div Setting DSO_CH1 V/Div: 2V/Div DSO_CH2 V/Div: 2V/Div
DSO_CH3 V/Div: 2V/Div DSO_CH4 V/Div: 2V/Div
Channel Setting
Channel Height Setting
DSO_CH1 Height: 80 DSO_CH2 Height: 80 DSO_CH3 Height: 80 DSO_CH4 Height: 80
Master
Logic Analyzer O DSO
DSO Settings OK Cancel Default Help



STEP 8. Select the connected DSO Manufacturer.

)scilloscope Brand:	Tektronix		7		
onnect Mode					
💽 USB	C TCP/I	P	CA	JTO	
🗖 Use the Agilent	GPIB-to-U	58 Switch	ning Car	d	
tack Parameters			000500520		
Current Connect Model:	TDS 100.	2B-SC		_	
Sampling Frequency:	100000.	00	Hz		
Stacking Delay:	0		Ps		
Trigger Position:	50		%		
Trigger Channel:	External	y.	1.00	-	V V
Trigger Type	1				-00
F Activate					
🖲 Trigger Edge	Rising Ed	lge 💌			
C Video	All Lines	-			
C Pulse	<	-	100		ns
Polarity: Nec	-	Upper L	.imit:	2.0	ns
Trig When: Out	side 🔻	Lower L	.imit;	2.0	ns
1000					_

STEP 9. Set the Connection Mode to USB or TCP/IP according to the connection mode of DSO. If selecting TCP/IP, it is necessary to key in the IP Address of current computer. Users also can select AUTO to auto-recognize the Online Mode.(Tektronix 1000,2000 series adopt the USB Interface to connect.)

Oscilloscope Brand:	Tektronix	7	
Connect Mode			
C LISE	C TCP/IP	C AUTO	_
	10F10-00000000	caning card	
5tack Parameters			
Current Connect Model:	TDS 1002B-SC	_	
Sampling Frequency:	100000.00	Hz	
Stacking Delay:	0	Ps	
Trigger Position:	50	%	
🗖 Trigger Channel:	External	1.00	۷
Trigger Type	- 22		
🗖 Activate			
💽 Trigger Edge	Rising Edge	-	
C Video	All Lines	2	
C Pulse	<	- 100	ns
Polarity: Nec	uppe	r Limit; 2.0	ns
Trig When: Out	side 🔻 Lowe	r Limit: 2.0	ns



STEP 10. It will display the currently connected DSO Model after pressing the Online button.

Settings			
Oscilloscope Brand:	Tektronix	7	
Connect Mode			
💽 USB	C TCP/IP	${f C}$ auto	
🗖 Use the Agilent	GPIB-to-USB Swit	ching Card	
itack Parameters			
Current Connect Model:	TDS 10028-SC		_
Sampling Frequency:	100000.00	Hz	
Stacking Delay:	0	Ps	_
Trigger Position:	50	%	
🗖 Trigger Channel:	External	. 1.00	۷ –
Trigger Type	<u></u>		- 102
Activate			
🖲 Trigger Edge	Rising Edge	-	
C Video	All Lines	3	
C Pulse	<	100	ns
Polarity: Nec	upper	: Limit; 2.0	ns
Trig When: Out	side 💌 Lower	Limit; 2.0	- ns

STEP 11. Set the relevant parameter and click the OK button.

Connect Mode			
C USB	${f C}$ TCP/IP	C AUTO	
🔲 Use the Agilent	GPIB-to-USB Sw	itching Card	
Stack Parameters			
Current Connect Model:	TDS 1002B-SC		
\square Sampling Frequency:	100000.00	Hz	
🔲 Stacking Delay:	0	Ps	
Trigger Position:	50	- %	
Trigger Channel:	External	▼ 1.00	۷ 🗌
Trigger Type	- 22		
C Activate			
🕑 Trigger Edge	Rising Edge	~	
C Video	All Lines	-	
C Pulse	<	- 100	ns
Polarity: Neo	g 💌 Uppe	er Limit; 2.0	ns
Trig When: Out	tside 🔽 Lowe	er Limit; 2.0	ns



STEP 12. Select DSO_CH1 and DSO-CH2 channels to analyzer A0, A1 channels of LA. Below is the waveform it

captured.

tall and the state		■ - 2.A	nn <u>st</u> X X 22 Br H Le Le M + 41 (22 - 24 Anglet 728 + Tragger De Thinne Forent Bin (72 - 1 Argine See See - Nov "N Dea First 22 Billion + A - F - 18 Billion + A - F - 18 Billion + Deaple Base - See "N Dea First 22 Billion + 1 - 7 + 18 Billion + Deaple Base Billion +	
Buillipil	Trigger	Filter	-then -then -then 🕐 -then 📕 then Alem Alem alem a	-
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050,040		4.4.4.4		
# A0	100.5		Unknown	
# A1 A1	11	-	Makrown	
	- 00	32 .	Britmens	
- A5 /1	- 22	1.52	Unknown	
* 44 ml	22	1.94	Unknown	
₹ 45 III	- 25	100	Italinetta	
# M. II.	- 10	S. BEL	Unknown	
# 47.11	- 10	134.	Bakaren	
* 10 11	8	20.	Unknown	
# # 0	35	31	Unknown	
# 82 E	-31	- 10	Unimoren	
- 83.11	35	(20)	Deknown	
# 84 35	- 22	1.12	Unknown	
		110	•	



5 Troubleshooting

- 5.1 Installation Troubleshooting
- 5.2 Software Troubleshooting
- 5.3 Hardware Troubleshooting



Objective

In this chapter, troubleshooting is divided into installation, software and hardware issues. These troubleshooting questions and answers depend not only on our engineers, but also on end users such as students, engineers, technical manual writers, and others.

5.1 Installation Troubleshooting

- Q1. Why it is not prompt when I insert the driver CD into my CD-ROM?
- A: At this stage, the driver CD is not auto-executable. The primary issue here is a chipset problem. Though these six Logic Analyzer models seem only different in model number, they are quite different in firmware and chipsets. Due to installation procedures (see *Chapter 2*), we are unable to compile a driver program that auto-detects the chipset at the beginning of the installation.
- Q2. Why does the installation software keep giving an error message saying that I don't have enough memory?
- A: This kind of problem happens in many hardware installations. Turn off multimedia programs such as Media Player, media decoders, media encoders, and so on. If there are any multimedia icons in the system tray (see the far right end of the **START** menu taskbar), remove them. The Logic Analyzer software will run better in memory locations from 64 to 512 MB.
- Q3. What should I do if I want to share this software interface with all users of my computer after installing it?
- A: The shortcut is removing the software interface, and then reinstalling it. By default, the program is available for all users.

Q4. My HDD is modest; which software components are absolutely necessary?

A: Choose **Custom** as your setup type. Next, unselect items such as examples and tutorials. You must install at least the Main App (application).

Q5. My MS Windows system will not accept the driver; what should I do?

A: Double check that you run the correct Setup.exe from the folder that corresponds to your hardware and MS Windows version. Visit our website for the latest updated or debugged software. If you are running this program on a virtual machine, the virtual machine may not support the amount of hardware addressing. In this case, try it with a machine that is physically running a Windows system.



5.2 Software Troubleshooting

Q1. Can I run the program even if I don't have the Logic Analyzer hardware?

A: Yes, you can. You can run the program under the demo mode. See. Fig5-1.

🧊 ZEROPLUS Logic Analyzer	x
Hardware Searching failed!	
Run Demo Retry Exit	

Fig. 5-1: Select **Run Demo** if you do not have the actual hardware.

- Q2. I am running a graphing program and software at the same time. Whenever I try to make a screenshot of my work, it keeps telling me that I have insufficient memory space; what is wrong?
- A: A few users have reported similar problems. We are not certain what causes it or how to fix it. However, we have found that if there is a defective address within 128 MB to 512 MB in your physical memory, your software might signal "End of memory". Thus, the program will warn you about insufficient memory. Test your memory with a varied memory testing program. Or, take a screenshot, close the program, paste it to the graphing program, and re-open the program.
- Q3. A part of the background picture remains within the Waveform Display Area, especially when running the program in demo mode. What's wrong with it?
- A: Your machine may have a memory management problem with either your physical RAM onboard or the RAM on your video card. Turn off any other multimedia of graphic programs and then re-run the software. If this does not work, restart your system. This should temporarily fix the problem. However, we highly recommend terminating all irrelevant programs while working with the Logic Analyzer (Try not to burn DVDs, not listen to music or watch movies while working with the Logic Analyzer.).
- Q4. The default color setting of the Waveform Display Area is very cool, but I don't see anything when I print my work out with my black and white laser printer. What can I do?
- A: Refer to Section 3.6; it should have clear, understandable instructions about changing the color of the user interface. See *Fig. 3-153*; this color setting should give a clear view of the Waveform Display Area, even with an old black and white laser printer.



5.3 Hardware Troubleshooting

Q1. Why are no lights on when I hook the USB cable to the Logic Analyzer?

A: Double check whether the other end is properly connected to your PC. There may also be a defect in your USB cable. Try another cable.

Q2. Why can't I read any signals from my Logic Analyzer?

A: Check whether you have correctly connected the signal cables to the activated pin on your test board and check the power supply of your test board. The Logic Analyzer does not supply any electricity to a test board via signal lines.

Q3. I get a signal from only one Logic Analyzer when I have two connected; what is wrong?

A: Currently, only the LAP-32128U-A, LAP-321000U-A, LAP-322000U-A, LAP-C(32128), LAP-C(321000) and LAP-C(322000) support many Logic Analyzers working in series. Also, make sure that the signal lines, power lines, and ground line are properly connected. Refer to Fig. *1-11, Table 1-2, Table 1-3, Table 1-4*, and *Table 1-5*.

Q4. Why should I bother grounding? Where can I ground?

A: Grounding will protect the Logic Analyzer and the test board. A proper ground may improve the quality and accuracy of your data. Since it is impossible to avoid unwanted interference you may ground the Logic Analyzer with the test board to ensure that unwanted interference will equally disturb both the testing and tested devices, ensuring a set of data that is still accurate.

Conclusion

Every user of a product is a potential writer for *Chapters* 5~7 in this User Manual. In fact, this chapter is a composition of many unnamed electronic professionals, especially experts.



6 FAQ

- 6.1 Hardware
- 6.2 Software
- 6.3 Registration
- 6.4 Technical Information
- 6.5 Others



Objective

In this chapter, common problems and questions are roughly classified into five categories: Hardware, Software, Registration, Technical Information, and Others. This is a backup resource for users, especially those without Internet access. Most references refer to English web links.

6.1 Hardware

H01. Is it ok to substitute stock items for bundled cables and connectors?

A: Yes, users may use any compatible connectors and cables. However, to ensure consistency and accuracy in measurements and data, we strongly recommend using the bundled connectors and cables. Each of the Logic Analyzer's is calibrated with the bundled cables and connectors before packing.

H02. Does Zeroplus manufacture grippers? How may I purchase grippers?

A: Yes, we have a production line dedicated to grippers. Contact our sales department and a sales representative will be happy to assist you.

H03. Is the memory size fixed? If I just use one of the ports, can I expand the memory size?

A: The Logic Analyzer's memory is fixed at 4 megabits. Due to current hardware limitations, the memory size cannot be modified, even as the number of ports used changes.

H04. Are different external sampling frequencies for different channels possible?

- A: No, there is only one external sampling frequency available.
- H05. Can I disable or set a certain port to don't care while during compression?
- A: No, during compression, D Port will be set to be **disabled**.

H06. Why does the Logic Analyzer feature negative voltage calibration?

A: This allows users to analyze any given signal.

H07. How do I adjust the Trigger Level?

A: The adjustment of the trigger level is done with a port which consists of 8 channels. The trigger lever can only be adjusted for an entire port.

H08. Does the Logic Analyzer use hardware or software compression technology?

A: For time efficiency, the Logic Analyzer uses hardware compression.

H09. Is planning an Analyzer that can handle more channels?

- A: Yes, we are working in this direction.
- H10. Does the memory page vary when the depth of the memory changes?
- A: Yes, the depth of memory changes the memory page.

H11. Is the Logic Analyzer expandable? How may I expand it?

A: Yes, the Logic Analyzer is expandable. At this stage, you can expand it with external module devices.

H12. Why must I reinstall the driver every time I use a different Logic Analyzer?

A: Since each Logic Analyzer has unique serial numbers, you must reinstall the driver every time you change the Logic Analyzer.

H13. Why is there no data? Why does data sampling seem inconsistent?

- A: The reasons are varied, but you may follow this checklist for troubleshooting:
 - 1) Always check the USB connection between the Logic Analyzer and your PC.
 - 2) We strongly recommend using USB ports in the rear panel of a PC; these ports usually have better voltage stabilities than front panel ports. However, if front panel USB ports are directly soldered to the main board, you can use them.
 - 3) Make sure the Logic Analyzer is directly connected with the PC (without a USB hub).
 - 4) Inconsistent data display may indicate voltage irregularities in the main board; examine capacitors on your main board or power supply.



5) If the problem is the power supply, we strongly recommend purchasing a power supply with a hardwired voltage transformer rather than a voltage regulator. For power supplies with the same output power, those built with hardwired voltage transformers are usually much heavier than those relying on voltage regulators.

H14. What are the time settings for "Setup" and "Hold"?

A: Setup Time: 0.05ns ~ 0.25ns; Hold Time: 0.02ns ~ 0.08ns.
 Clock High requires a minimum of 0.31ns. Clock Low requires at least 0.47ns.



6.2 Software

SW01. Why is the compression function not enabled by default?

A: Mostly to avoid significant errors when testing signals with high variability, or measuring a certain channel for a long time period.

SW02. What is the purpose of the compression function?

A: The compression function measures signals that vary slightly over a long period.

SW03. Can I enable Trigger Page and Compression Function simultaneously?

A: Yes, you can.

SW04. When should I use the "Bar" function?

A: This function allows you to highlight a segment of a waveform so that you can have a closer view. Depending on the configuration of **Waveform Display Mode** under **Tools** → **Customize**, a more accurate numeric value of sampling site, time, or frequency difference will be calculated and displayed as shown in *Fig. 6-1*.

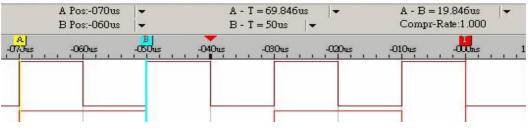


Fig. 6-1 - Bar Function

SW05. Can triggers be differentiated in Pre-Trigger and Post-Trigger?

A: Yes, they can.

SW06. Are all setup parameters and configurations saved as I save my work?

- A: Yes, everything in your work space, except signal graph, will be saved.
- SW07. If I have the wheel feature with my mouse (or other pointing devices), may I adjust the waveform display zoom, in the Waveform Display Mode by scrolling?
- A: This feature has been enhanced since V1.03. If your program version is prior to this version, visit our website for the latest update at

http://www.zeroplus.com.tw/logic-analyzer en/technical support.php

SW08. What are the extremes for Delay Time and Clock & Trigger Delay Clock?

A: The interface will inform you of the interval you may use. However, it varies from case to case, depending on your test devices. See *Fig.* 6-2.

Delay Time and Clock Trigger Delay Time
5ns
(Min:5ns , Max:83.880955ms)
Trigger Delay Clock
1
(Min:1,Max:16776191)

Fig. 6-2 - Delay Time and Clock

SW09. How do I know the version number of my software interface program?

A: Click Help from the menu (See Fig 6-3), and then select About ZEROPLUS Logic Analyzer(See Figs 6-3 and 6-4).



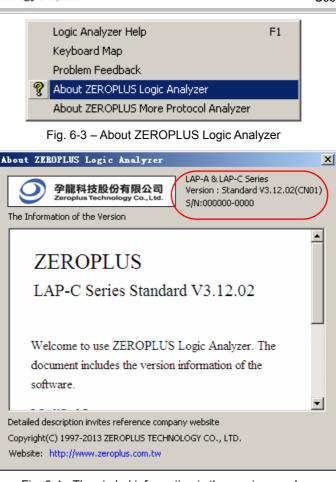


Fig. 6-4 - The circled information is the version number.

SW10. How may I upgrade my software interface program?

A: Visit our website at <u>http://www.zeroplus.com.tw</u> and follow the instructions for the English version. You may also use the following address for English updates. <u>http://www.zeroplus.com.tw/logic-analyzer_en/technical_support.php</u>

SW11. Can I save my signal data to a separate pure text file (*.txt)?

A: This feature is available in this version.

SW12. Why is the text display covered by other text or outside the display width?

A: At this stage, our software interface program has missing code for multilingual support. You will have to ensure your system default encoding is one of the following languages: 1) any English Encoding (en, en-XX), 2) Traditional Chinese (zh, zh-XX), 3) Simplified Chinese (zh, zh-CN in HZ, GB2312, GB18030). Double check the language configuration in **Regional and Language Options**.



Fig.6-5 – Windows Regional and Language Options

SW13. Is there a Reset that restores the default color settings for signal output waveforms in the Position Signal Display Area?

A: Yes, there is. Click **Tools** from the menu bar, and select **Color Setting**; click **Defaults**. However, this restores everything in this window. You must make a further adjustment if the color setting is the only thing you want to

② 孕龍科技股份有限公司 Zeroplus Technology Co., Ltd.

restore. See Fig. 6-6.

Name	Relating	Color	
Waveform Background		000	
List Background 1	Ē		
List Background 2	Π		1
Cursor			1
Grid			
Unknown Line			
Default Bus			
Bus Text			
List Text			
Time Text			<u> </u>
Bus Error			
Bus Error Text			
Signal Filter Bar			
Preview	0 0 0	1 altered, cor automatical according t ratio.	o the contrast

Fig. 6-6 - Restore Color Defaults

SW14. Can I change the displayed waveform mode?

A: Yes, you can. There are two ways to do this. First, go through Data → Waveform Mode and choose a waveform. See Fig. 6-7.

	Select an Analytic Range Noise Filter Bus Width Filter Data Contrast				
两	Find Data Value	Ctrl+F			
	Find Pulse Width				
1+	To the Previous Edge	F11			
* [To the Next Edge	F12			
	Go To		۲	1	
Bar	Add Bar	Alt+A			
- 2 Bar	Delete Bar	Alt+B			
N	Zoom	E			
en	Hand	н			
R	Normal	ESCAPE			
ллı Қ	Zoom In	F9			
K	Zoom Out	F8			
	Show all Data	F10			
5	Previous Zoom	Ctrl+Z			
	Data Format		۲		
	Waveform Mode		Þ	~	Square Waveform
	List Data Mode		۲		Sawtooth Waveform

Fig. 6-7 – Waveform Mode

The second alternative is to right-click any place in the Waveform Display Area. Then, a menu will pop up. Click **Waveform Mode**, and choose a waveform. *See Fig. 6-8.*



Color Bus Data Color		Г	Sawtooth Waveform
Waveform Mode	•	•	Square Waveform
Data Format	•		
Previous Zoom	Ctrl+Z		
Show all Data	F10		
Normal	ESCAPE		
Hand	н		
Zoom	E		
Add Bar			
Place	•		
Go To	•		
	Place Add Bar Zoom Hand Normal Show all Data Previous Zoom Data Format Waveform Mode Color	Find Pulse Width Go To Place Add Bar Zoom E Hand H Normal ESCAPE Show all Data F10 Previous Zoom Ctrl+2 Data Format Waveform Mode Color	Find Pulse Width Go To Place Add Bar Zoom Hand Hand Hand Hand H Normal ESCAPE Show all Data F10 Previous Zoom Ctrl+Z Data Format Waveform Mode ▼ Color

Fig.6-8 – Waveform Mode

SW15. Can I change the Signal Display Mode into the Timing Mode?

A: Yes, you can.

SW16. Why does not Filter Delay work when the Double Mode is enabled?

A: To optimize signal output quality and maximize memory efficiency, the **Signal Filter Setup** function may work under the Double Mode. However, the **Filter Delay** function doesn't work under the Double Mode at this stage.



6.3 Registration

RG01. What is the significance of the hardware serial number?

A: Every product is assigned and engraved with a unique serial number, which allows us to trace the original manufacturing date of a specific product.

RG02. How do I register online?

A: Visit our homepage at http://www.zeroplus.com.tw. Choose the Instrument Department, and click on English. Once you finish membership registration, proceeding with product registration. After finishing product registration, you will receive an email consisting of your product registration information. A password may be required for further customer services and other inquiries.

RG03. What should I do if online registration fails?

A: Do a screen grab of the window, including the error message, and email our customer service dept. A customer service representative will be glad to assist you as soon as possible once the email is correctly received.

RG04. How may I register if the purchasing date was more than one month ago?

A: In this case, fill in the registration card and send it via post, fax, or email to our customer service dept ,and a representative will process the registration for you.

RG05. What is the warranty length for my product?

A: A two-year FACTORY WARRANTY is offered in which you will have to send the defective product to the closest branch, an authorized service site, or our headquarters. The in-store warranty may vary, and many require extra charges for various extended warranty policies. The company is not being responsible for an in-store warranty that exceeds our factory warranty.

RG06. Why should I register this product?

A: If you do not register this product, the warranty will be counted from the manufacturing date indicated by the serial number of your product. Thus, we strongly recommend registering your product for your own benefit.

RG07. What should I do if the hardware serial number is previously registered?

A: In this case, take a picture of the decal on the rear side of the product and fill in the registration form. Call us and mail both picture and registration to us. A customer representative will be happy to assist you.

RG08. How do I register the protocol analyzer and buy protocols?

A: Every product is assigned and engraved with a unique serial number. please print your S/N number window as an example attachment and send it to our distributor or ZEROPLUS head office. According to your S/N, we will provide passwords for your protocol registration.



6.4 Technical Information

TI01. What is the Logic Analyzer?

A: The Logic Analyzer is a tool that sieves out and shows the digital signal from test equipment by using a clock pulse. The Logic Analyzer is like a digital oscilloscope. However, it only shows two voltage states (the logic status 1 and 0), differing from many voltage levels of an oscilloscope. The Analyzer has more channels than an oscilloscope to analyze the waveform. Since the Logic Analyzers obtains only signals 1 and 0, its sampling frequency is slower than an oscilloscope, which needs many voltage ranks. Moreover, the Logic Analyzer can receive many signals during a test.

TI02. How does the Logic Analyzer operate?

A: The Logic Analyzer reserves trigger requirement setting for users and uses them on the test equipment for the value of the sampling signals and puts them into the internal memory. The software of the Logic Analyzer will read out the value from the memory and switch it to the waveform or status shown for users' analysis.

TI03. What is the asynchronous Timing Mode?

A: Since the sampling clock and tested objects are not directly related to each other, and the former won't be controlled by the latter, the sampling clock and the tested signals will not be done at the same time. We call this "Timing Mode", which means that in the same time interval, you can get sampling data from the test equipment at one time, such as every 10 seconds. The internal clock, the Logic Analyzer's inner confirmed one, is often for sampling in Timing Mode as is the logic waveform.

TI04. What is the synchronous State Mode?

A: Because the sampling clock and measured object can be directly related, and are controlled by the latter, signals of the former and the latter can proceed simultaneously. We call this "State Mode". In this mode, the measured object provides the sampling clock. State Mode is when the Logic Analyzer can obtain sampling data from the test equipment synchronously. In other words, when the test equipment has a signal or signal group, this is the time to get the signal. For example, while the test equipment is sending out one rising edge, the Logic Analyzer can start to obtain one signal.

TI05. What are A-bar, B-bar and T-bar?

A: The T-bar, A-bar and B-bar are labels. T is the trigger label, which cannot be removed when the waveform or the state is displayed, which marks a pod. When searching for, or obtaining data, the A and B labels can be set in any location. Using the order of these markings, you can return quickly to the desired position to analyze data. This can also be a point to measure the interval between A-B, A-T, or B-T.

TI06. What is a Trigger Gripper?

A: A gripper is the gathering point to collect the Logic Analyzer channels. When a cable connector is not suitable for the test device, a trigger gripper may be an alternative for connection.

TI07. What is a Channel?

- A: The channel is the collection line of the input signal. Each channel is responsible for linking the pin of the measured device. Every channel is used to collect signals from the test equipment.
- TI08. How can I display acquisition in the waveform captured by external sampling signal?
- A: Select Waveform Display from the Window list.

TI09. What is an External Trigger?

A: An external trigger is a signal outside the Logic Analyzer. It is used for the simultaneous test of 2 test tools. For example, one Logic Analyzer can be started by one signal from another test tool. Or when it is triggered, it can output one signal to another test tool. The Logic Analyzer is often used for triggering an oscilloscope.

TI10. Why does Double Mode not coincide with Filter Delay?

A: In order to set out the perfect waveform from the Logic Analyzer and achieve optimal memory efficiency, you can use the **Signal Filter** when using **Double Mode**; the system doesn't support the function of **Filter Delay**.

TI11. How do I update software?

A: The software will automatically check for and download updates. This function deletes old software first and then downloads and installs the latest version.



6.5 Others

OT01. How was the Logic Analyzer developed?

A: It took us more than two years to develop this product. We envision "Everyone carrying the Logic Analyzer," and we would like to make some contributions to the electronics industry in return. We also wish to transform the stereotypical OEM factory into a world class R&D center.

OT02. Why is there a rich information database for game chips rather than the Logic Analyzer?

A: First of all, we apologize for any inconvenience caused by the lack of information pertaining to Logic Analyzers. We are currently working very hard on multilingual information and documentations pertaining to the Logic Analyzer. Visit our website for the latest drivers, software, and manuals: http://www.zeroplus.com.tw/logic-analyzer_en/technical_support.php. In the meantime, we will have updates ready when verified error free.

OT03. What was the original intention of developing this item?

A: Originally, the Logic Analyzer was just for use by our engineering department. Later on, we saw the greater need for this kind of device. We made numerous enhancements and made it available to the public.

Conclusion

This chapter is full of hard facts for engineers. The contents of this version of the User Manual may look more different than the one on the web. Every engineer finds new problems, new solutions, or other issues, during real life applications. Though there are dozens of questions here, we look forward to your feedback, which is important for future versions. It may help us produce more efficient and accurate devices so that we will offer you much better service.



7 Appendix

- 7.1 Hot Keys
- 7.2 Contact Us



Objective

In this chapter, users will learn the functions of all defined hot keys in the software interface of the Logic Analyzer.

7.1 Hot Keys

Hot Key	Equivalent Orders	Statement
А	Go to A Bar	Move the A-bar to the center of the waveform area; select A-bar by the cursor.
В	Go to B Bar	Move the B-bar to the center of the waveform area; select B-bar by the cursor.
Т	Go to T Bar	Move the T-bar to the center of the waveform area; select T-bar by the cursor.
E	Change to Zoom mode	Change the mouse mode to Zoom
Н	Change to Hand mode	Change the mouse mode to Hand.

Table 7-1: Hot Keys (1)

Table 7-2 : Hot Keys (2)

Hot Key	Equivalent Orders	Statement			
Ctrl + A	Go to A Bar	Center A-bar.			
Ctrl + B	Go to B Bar	Center B-bar.			
Ctrl + C	File -> Capture Window	Open Capture Graph dialog box.			
Ctrl + E	Data ->Zoom	Change Mouse mode to Zoom mode.			
Ctrl + F	Data -> Find Data Value	Search specific data with predetermined conditions.			
Ctrl + G	Bus/Signal -> Group into Bus	Group selected signals into a Bus.			
Ctrl + N	File -> New	Create a new file.			
Ctrl + O	File -> Open	Open a saved file.			
Ctrl + P	File -> Print	Print an active file.			
Ctrl + S	File-> Save	Save an active file with its current name, location and file format.			
Ctrl + U	Bus/Signal -> Ungroup from Bus	Ungroup signals (Pins) from a Bus.			
Ctrl + Z	Data -> Previous Zoom	Reverse the last zoom.			
Ctrl + Shift + E	File->Export Waveform	Open Export Waveform dialog box.			

Table	7-3	:	Hot	Keys	(3)
-------	-----	---	-----	------	-----

Hot Key	Equivalent Orders	Statement
Page Down	Operate the position shown	Go to next page of the data or the waveform
Page Up	Operate the position shown	Go to previous page of the data or the waveform
Home	Operate the position shown	Go to the beginning of the data or the waveform
End	Operate the position shown	Go to the end of the data or the waveform.
Up	Operate the position shown	Move the cursor up a grid.
Down	Operate the position shown	Move the cursor down a grid.
Left	Operate the position shown	Move the selected Bar or display left to prior the waveform or data.
Right	Operate the position shown	Move the selected Bar or display right to posterior the waveform or data.
ESC	Operate the position shown	Release all selected bars, and change Mouse mode to Normal.
Space	Change the trigger conditions	Change trigger conditions.



Table	7-4	:	Hot	Keys	(4)
-------	-----	---	-----	------	-----

Hot Key	Equivalent Orders	Statement
F1	Help -> Logic Analyzer Help	Logic Analyzer Help
F2	Decrease the sampling rate	Decrease the sampling rate
F3	Increase the sampling rate	Increase sampling rate
F5	Run/Stop -> Single Run	Execute the acquirement once
F6	Run/Stop -> Repetitive Run	Execute the acquirement continuously
F7	Run/Stop -> Stop	Stop acquiring data
F8	Data -> Zoom Out	Zoom out the waveform
F9	Data -> Zoom In	Zoom in the waveform
F11	Data ->To the Previous Edge	Move forward to the prior variation waveform and center that location.
F12	Data -> To the Next Edge	Move forward to the next variation waveform and center that location.



7.2 Contact Us

Table 7-5: Contact Us

Contact Us					
Copyright 1997-2012, ZEROPLUS TECHNOLOGY CO., LTD					
Headquarter					
	ZEROPLUS TECHNOLOGY CO., LTD.				
	3F., No.121, Jian Ba Rd.,				
Taiwan Chung Ha City	Chung Ho City, Taipei County, R.O.C.				
Taiwan-Chung Ho City	Tel: +886-2-6620-2225				
	Fax: +886-2-6620-2226				
	ZIP Code: 23585				
Instrument Division/ Business Department					
	ZEROPLUS TECHNOLOGY CO., LTD.				
	2F., No.242-1, Nanya St., North Dist.,				
	Hsinchu City 30052, Taiwan (R.O.C.)				
Taiwan-Hsinchu City	Tel: +886-3-542-6637 / Ex 87				
	Fax: +886-3-542-4917				
	ZIP Code: 30052				
	E-Mail: hunter@zeroplus.com.tw				
	ZEROPLUS TECHNOLOGY CO., LTD.				
	Address: 2F, NO.123, Jian Ba Rd,				
Taiwan-Chung Ho City	Chung Ho City, Taipei Hsian, R.O.C.				
	Tel: 886-2-6620-2225				
	Fax: 886-2-2223-4362				
	E-mail: service_2@zeroplus.com.tw				
Other Service					
Departments					
	ZEROPLUS TECHNOLOGY (DONG GUAN) CO,.				
	LTD				
	Room 402, Block D, Building 13, Courtyard 9(Dangdai				
China-Beijing	Chengshi Jiayuan), Anningzhuang West Road, Haidian				
China Doijing	District, Beijing				
	Tel: +86-10-51159268				
	Fax: +86-10-51159278				
	ZIP Code: 100085				



	E-Mail: adam1833@zeroplus.com.tw				
	kan@zeroplus.com.tw				
	ZEROPLUS TECHNOLOGY (DONG GUAN) CO,.				
	LTD.				
	Room 605, Building C, Area A, Huameiju Commercial				
	Center, Xinhu Road, Bao'an 82 District, Shenzhen				
China-Shenzhen	Tel: +86-755-2955-6305				
	Fax: +86-755-2955-6306 #613				
	ZIP Code: 518000				
	E-Mail: jesse_cn@zeroplus.com.tw				
	kan@zeroplus.com.tw				
	ZEROPLUS TECHNOLOGY (DONG GUAN) CO,.				
	LTD.				
	Room 101, 8 th Building, Lane 825, Chenghui Road,				
	Zhangjiang District, Pudong New Area, Shanghai City				
China-Shanghai	Tel: +86-21-50155235~6				
	Fax: +86-21-50155235 #607				
	ZIP Code: 201203				
	E-Mail: adam1833@zeroplus.com.tw				
	kan@zeroplus.com.tw				

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Conclusion

The demonstrations in this User Manual will enhance users' understanding on our products in future issues, even though the manual ends here. Thank you for choosing our Logic Analyzer. Please contact us if you find anything that could be done better, about either software or hardware. We appreciate your feedback.