



SPECTRUM

SYSTEMENTWICKLUNG MICROELECTRONIC GMBH

MX.40xx - 14 bit PXI transient recorder

- **PXI 3U / CompactPCI 3U format**
- **Fastest 14 bit A/D converter board**
- **Models with 20 MS/s or 50 MS/s**
- **1 or 2 channels acquisition**
- **Simultaneous sampling on all channels**
- **6 input ranges: ± 200 mV up to ± 10 V**
- **Up to 64 MSample memory**
- **FIFO mode**
- **Window and pulsewidth trigger**
- **Input offset up to $\pm 200\%$**
- **Synchronization possible**
- **Windows program SBench 5.x included**



Product range overview

Model	1 channel	2 channels	4 channels
MX.4020	20 MS/s		
MX.4021	20 MS/s	20 MS/s	
MX.4030	50 MS/s		
MX.4031	50 MS/s	50 MS/s	

Software/Drivers

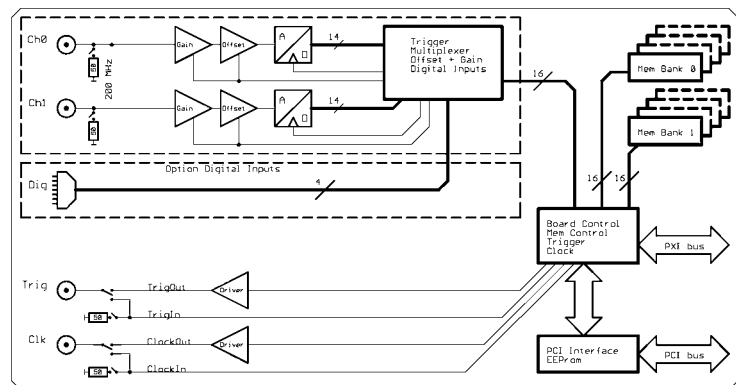
A large number of drivers and examples are delivered with the board or are available as an option:

- Windows 98/ME/NT/2000/XP - drivers
- Linux - drivers
- SBench 5.2
- Streaming Software SPviewIT 6.2(as option)
- Visual C++/Borland C++ Builder examples
- Borland Delphi examples
- Microsoft Visual Basic examples
- Microsoft Excel examples
- LabWindows/CVI examples
- FlexPro support with SBench
- LabVIEW - drivers (as option)
- DASyLab - drivers (as option)
- MATLAB - drivers (as option)
- Agilent VEE - drivers (as option)

General Information

The MX.40xx is best suitable for applications that need high samplerates as well as a maximum signal dynamic. These boards offer a resolution 4 times higher than 12 bit boards. On the MX.40xx every channel has its own amplifier and A/D converter. Each input channel could be adapted to a wide variety of signal sources. This is done by software selecting a matching input range, an input impedance and an individual input offset. The user will find easily a matching solution from the six offered models. These versions are working with samplerates of 20 MS/s or 50 MS/s and have one or two channels and could also be updated to a multi-channel system using the internal synchronization bus. Data is written in the internal 8 MSamples up to 64 MSample large memory. This memory could also be used as a FIFO buffer. In FIFO mode data could be transferred on-line directly into the PC RAM or to hard disk.

Hardware block diagram



Software programmable parameters

Samplerate	1 kS/s to max samplerate, external clock, ref clock, PXI clock
Input Range	± 200 mV, ± 500 mV, ± 1 V, ± 2 V, ± 5 V, ± 10 V
Input impedance	50 Ohm / 1 MOhm
Input Offset	$\pm 200\%$ in steps of 1%
Clock mode	internal PLL, internal quartz, external, external divided, external reference clock, PXI reference clock
Clock impedance	50 Ohm / 1 MOhm
Trigger impedance	50 Ohm / 1 MOhm
Trigger mode	Channel, External, Software, Auto, Windows, Pulse, PXI Line[5..0], PXI Startrigger
Trigger level	1/1024 to 1023/1024 of input range (10 bit)
Trigger edge	rising edge, falling edge or both edges
Trigger pulsewidth	1 to 255 samples in steps of 1 sample
Memory depth	32 up to installed memory in steps of 32
Posttrigger	32 up to 128 M in steps of 32
Multiple Recording segmentsize	32 up to installed memory / 2 in steps of 32

Possibilities and options

PXI bus

The PXI bus (PCI eXtension for instrumentation) offers a variety of additional normed possibilities for synchronising different components in one system. It is possible to connect several Spectrum cards with each other as well as to connect a Spectrum card with cards of other manufacturers.

PXI reference clock

The card is able to use the 10 MHz reference clock that is supplied by the PXI system. Enabled by software the PXI reference clock is feeded in the on-board PLL. This feature allows the cards to run with a fixed phase relation.

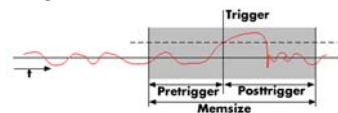
PXI trigger

The Spectrum cards support star trigger as well as the PXI trigger bus. using a simple software command one or more trigger lines can be used as trigger source. This feature allows the easy setup of OR connected triggers from different cards.

Input impedance

All inputs could individually be switched by software between 50 Ohm and 1 MOhm input impedance. If using fast signals and high sampling rates or have 50 Ohm cable impedance the use of the 50 Ohm termination is recommended to minimise noise and signal reflections. If using weak signal sources or standard probes the use of the 1 MOhm termination is helpful.

Ring buffer mode



The ring buffer mode is the standard mode of all oscilloscope boards. Data is written in a ring memory of the board until a trigger event is

detected. After the event the posttrigger values are recorded. Because of this continuously recording into a ring buffer there are also samples prior to the trigger event visible: Pretrigger = Memsize - Posttrigger.

FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The control of the data stream is done automatically by the driver on interrupt request.

Channel trigger

The data acquisition boards offer a wide variety of trigger modes. Besides the standard signal checking for level and edge as known from oscilloscopes it's also possible to define a window trigger. All trigger modes could be combined with the pulsewidth trigger. This makes it possible to trigger on signal errors like too long or too short pulses.

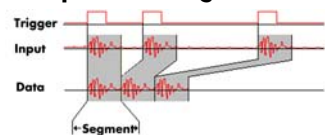
External trigger I/O

All boards can be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulse width. An internally recognised trigger event can - when activated by software - be routed to the trigger connector to start external instruments.

Pulse width

Defines the minimum or maximum width that a trigger pulse must have to generate a trigger event. Can be combined with channel trigger, pattern trigger and external trigger.

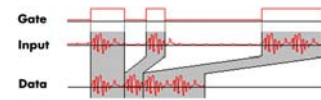
Multiple Recording



The Multiple Recording option allows the recording of several trigger events without restarting the hardware. With this option very fast repetition rates could be achieved. The

on-board memory is divided in several segments of same size. Each of them is filled with data if a trigger event occurs.

Gated Sampling



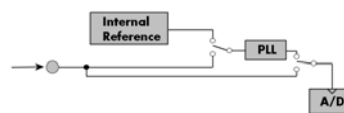
The Gated Sampling option allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level.

level.

External clock I/O

Using a dedicated connector a sampling clock can be fed in from an external system. It's also possible to output the internally used sampling clock to synchronise external equipment to this clock.

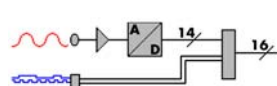
Reference clock



The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronise the board for high-quality mea-

surements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Digital inputs



This option acquires additional synchronous digital channels phase-stable with the analog data. When the option is installed there are 2 additional digital inputs for every analog A/D channel.

Technical Data

Resolution	14 bit	Dimension	160 mm x 233 mm (Standrad 6U)
Differential linearity error	± 0.5 LSB typ. (ADC)	Width (Standard)	1 slot
Integral linearity error	± 1 LSB typ (ADC)	Width (with digital inputs)	2 slots
Multi: Trigger to 1st sample delay	fixed	Width (with star hub option)	2 slots
Multi: Recovery time	< 20 samples	Analogue Connector	3 mm SMB male
ext. Trigger accuracy	1 Sample	Digital Connector	40 pol half pitch (Hirose FX2 series)
int. Trigger accuracy	1 Sample	Digital Inputs delay to analog sample	-6 samples
Ext. clock: delay to internal clock	42 ns ± 2 ns	Overvoltage protection (range ≤ ±1 V)	±5 V
input signal with 50 W termination	max 5 V rms	Overvoltage protection (range > ±1 V)	±50 V
Trigger output delay	1 Sample	Warm up time	10 minutes
Input impedance	50 Ohm / 1 MOhm 25 pF	Operating temperature	0°C - 50°C
Crosstalk 1 MHz sine signal 50 Ohm	< -80 dB	Storage temperature	-10°C - 70°C
Crosstalk 1 MHz sine signal 1 MOhm	< -65 dB	Humidity	10% to 90%
Min internal clock	1 kS/s	Zero offset error	adjustable by user
Min external clock	500 kS/s	Gain error	< 1 % of full scale
		Power consumption 5 V @ full speed	max. 2.6 A (13.0 Watt)
		Power consumption 5 V @ power down	max. 1.8 A (9.0 Watt)
Trigger input:Standard TTL level	Low: -0.5 > level < 0.8 V High: 2.0 V > level < 5.5 V Trigger pulse must be valid ≥ 2 clock periods.	Clock input: Standard TTL level	Low: -0.5 V > level < 0.8 V High: 2.0 V > level < 5.5 V Rising edge. Duty cycle: 50% ± 5%
Trigger output	Standard TTL, capable of driving 50 Ohm. Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA) One positive edge after the first internal trigger	Clock output	Standard TTL, capable of driving 50 Ohm Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA)

	MX.4020 MX.4021	MX.4030 MX.4031
max internal clock	20 MS/s	50 MS/s
max external clock	20 MS/s	50 MS/s
-3 dB bandwidth	> 10 MHz	> 25 MHz
Zero noise level at 50 Ohm	< 2.1 LSB rms	< 2.9 LSB rms

Dynamic Parameters

	MX.4020 MX.4021	MX.4030 MX.4031
Test - Samplerate	20 MS/s	50 MS/s
Testsignal frequency	1 MHz	1 MHz
SNR (typ)	> 69.7 dB	> 66.9 dB
THD (typ)	< -71.5 dB	< -70.8 dB
SFDR (typ), incl harm.	> 79.8 dB	> 73.8 dB
SINAD (typ)	> 67.5 dB	> 65.4 dB
ENOB (based on SINAD)	> 10.9	> 10.6

Dynamic parameters are measured at ± 1 V input range (if no other range is stated) and 50 Ohm termination with the samplerate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave of the specified frequency with > 99% amplitude. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits. For a detailed description please see application note 002.

Order information

Order No	Description	Order No	Description
MX4020	MX.4020 with 8 MSample memory and drivers/SBench 5.x	MX4xxx-16M	Option: 16 MSample memory instead of 8 MSample standard mem
MX4021	MX.4021 with 8 MSample memory and drivers/SBench 5.x	MX4xxx-32M	Option: 32 MSample memory instead of 8 MSample standard mem
MX4030	MX.4030 with 8 MSample memory and drivers/SBench 5.x	MX4xxx-64M	Option: 64 MSample memory instead of 8 MSample standard mem
MX4031	MX.4031 with 8 MSample memory and drivers/SBench 5.x	MX4xxx-up	Additional handling costs for later memory upgrade
MX4xxx-mr	Option Multiple Recording: Memory segmentation	MX40xx-dl	DASYLab driver for MX.40xx series
MX4xxx-gs	Option Gated Sampling: Gate signal controls acquisition	MX40xx-hp	VEE driver for MX.40xx series
MX40xx-dig	Additional 4 synchronous digital inputs per channel, incl. cable	MX40xx-lv	LabVIEW driver for MX.40xx series
		MATLAB	MATLAB driver for all MI.xxxx, MC.xxxx and MX.xxxx series.
Cab-3f-9m-80	Adapter cable: SMB female to BNC male 80 cm	Cab-3f-9f-80	Adapter cable: SMB female to BNC female 80 cm
Cab-3f-9m-200	Adapter cable: SMB female to BNC male 200 cm	Cab-3f-9f-200	Adapter cable: SMB female to BNC female 200 cm

technical changes and printing errors possible