



SPECTRUM

SYSTEMENTWICKLUNG MICROELECTRONIC GMBH

MX.31xx - 4 channel 12 bit A/D up to 25 MS/s

- **PXI 3U / CompactPCI 3U format**
- **12 bit A/D converter board**
- **1 MS/s, 10 MS/s or 25 MS/s**
- **2 or 4 channels per board**
- **Simultaneously sampling on all channels**
- **8 input ranges: ± 50 mV up to ± 10 V**
- **Up to 64 MSample memory**
- **FIFO mode to RAM or hard disk**
- **Window and Pulsewidth trigger**
- **Input offset up to $\pm 100\%$**
- **Synchronization possible**
- **Windows program SBench 5.x included**



Product range overview

Model	1 channel	2 channels	4 channels
MX.3110	1 MS/s	1 MS/s	
MX.3111	1 MS/s	1 MS/s	1 MS/s
MX.3120	10 MS/s	10 MS/s	
MX.3121	10 MS/s	10 MS/s	10 MS/s
MX.3130	25 MS/s	25 MS/s	
MX.3131	25 MS/s	25 MS/s	25 MS/s

Software/Drivers

A large number of drivers and examples are delivered with the board or are available as an option:

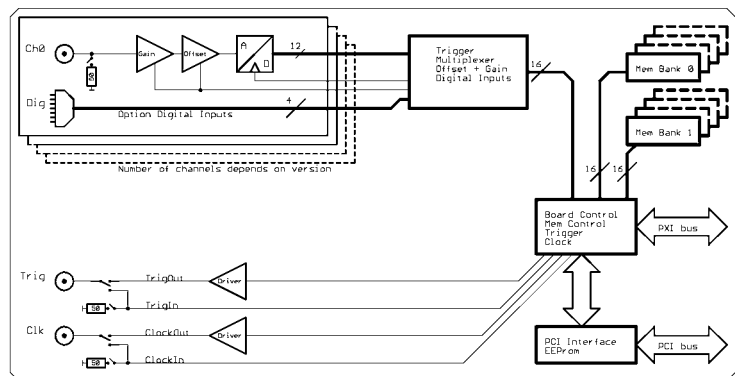
- Windows 98/ME/NT/2000/XP - drivers
- Linux - drivers
- SBench 5.2
- Streaming Software SPviewIT 6.2(as option)
- Visual C++/Borland C++ Builder examples
- Borland Delphi examples
- Microsoft Visual Basic examples
- Microsoft Excel examples
- LabWindows/CVI examples
- FlexPro support with SBench
- LabVIEW - drivers (as option)
- DASyLab - drivers (as option)
- MATLAB - drivers (as option)
- Agilent VEE - drivers (as option)

General Information

The MX.31xx series allows recording of two or four channels with samplerates of 1 MS/s, 10 MS/s or 25 MS/s. Due to the proven design a wide variety of 12 bit A/D converter boards for PXI bus could be offered. These boards are available in several versions and different speed grades making it possible for the user to find an individual solution.

As an option 4 digital inputs per channel could be recorded synchronously. The installed memory of up to 64 MSample will be used for fast data recording. It can completely be used by the currently active channels. If using slower samplerates the memory is switched to a FIFO buffer and data will be transferred on-line to the PC memory or to hard disk.

Hardware block diagram



Software programmable parameters

Samplerate	1 kS/s to max samplerate, external clock, ref clock, PXI clock
Input Range	± 50 mV, ± 100 mV, ± 200 mV, ± 500 mV, ± 1 V, ± 2 V, ± 5 V, ± 10 V
Input impedance	50 Ohm / 1 MOhm
Input Offset	$\pm 100\%$ in steps of 1%
Clock mode	internal PLL, internal quartz, external, external divided, external reference clock, PXI reference clock
Clock impedance	50 Ohm / 1 MOhm
Trigger impedance	50 Ohm / 1 MOhm
Trigger mode	Channel, External, Software, Auto, Windows, Pulse, PXI Line[5..0], PXI Startrigger
Trigger level	1/256 to 255/256 of input range
Trigger edge	rising edge, falling edge or both edges
Trigger pulsewidth	1 to 255 samples in steps of 1 sample
Memory depth	32 up to installed memory in steps of 32
Posttrigger	32 up to 128 M in steps of 32
Multiple Recording segmentsize	32 up to installed memory / 2 in steps of 32

Possibilities and options

PXI bus

The PXI bus (PCI eXtension for instrumentation) offers a variety of additional normed possibilities for synchronising different components in one system. It is possible to connect several Spectrum cards with each other as well as to connect a Spectrum card with cards of other manufacturers.

PXI reference clock

The card is able to use the 10 MHz reference clock that is supplied by the PXI system. Enabled by software the PXI reference clock is feeded in the on-board PLL. This feature allows the cards to run with a fixed phase relation.

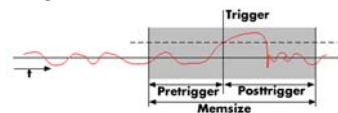
PXI trigger

The Spectrum cards support star trigger as well as the PXI trigger bus. using a simple software command one or more trigger lines can be used as trigger source. This feature allows the easy setup of OR connected triggers from different cards.

Input impedance

All inputs could individually be switched by software between 50 Ohm and 1 MOhm input impedance. If using fast signals and high sampling rates or have 50 Ohm cable impedance the use of the 50 Ohm termination is recommended to minimise noise and signal reflections. If using weak signal sources or standard probes the use of the 1 MOhm termination is helpful.

Ring buffer mode



The ring buffer mode is the standard mode of all oscilloscope boards. Data is written in a ring memory of the board until a trigger event is

detected. After the event the posttrigger values are recorded. Because of this continuously recording into a ring buffer there are also samples prior to the trigger event visible: Pretrigger = Memsize - Posttrigger.

FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The control of the data stream is done automatically by the driver on interrupt request.

Channel trigger

The data acquisition boards offer a wide variety of trigger modes. Besides the standard signal checking for level and edge as known from oscilloscopes it's also possible to define a window trigger. All trigger modes could be combined with the pulsewidth trigger. This makes it possible to trigger on signal errors like too long or too short pulses.

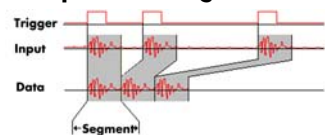
External trigger I/O

All boards can be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulse width. An internally recognised trigger event can - when activated by software - be routed to the trigger connector to start external instruments.

Pulse width

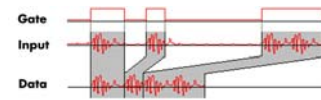
Defines the minimum or maximum width that a trigger pulse must have to generate a trigger event. Can be combined with channel trigger, pattern trigger and external trigger.

Multiple Recording



The Multiple Recording option allows the recording of several trigger events without restarting the hardware. With this option very fast repetition rates could be achieved. The on-board memory is divided in several segments of same size. Each of them is filled with data if a trigger event occurs.

Gated Sampling

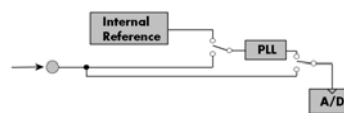


The Gated Sampling option allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level.

External clock I/O

Using a dedicated connector a sampling clock can be fed in from an external system. It's also possible to output the internally used sampling clock to synchronise external equipment to this clock.

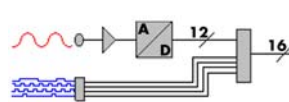
Reference clock



The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronise the board for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way.

The driver automatically generates the requested sampling clock from the fed in reference clock.

Digital inputs



This option acquires additional synchronous digital channels phase-stable with the analog data. When the option is installed there are 4 additional digital inputs for every analog A/D channel.

Technical Data

Resolution	12 bit	Dimension	160 x 100 mm (Standard 3U)
Differential linearity error	≤ 1 LSB (ADC)	Width (Standard)	1 slot
Integral linearity error	≤ 2.5 LSB (ADC)	Width (with digital inputs)	2 slots
Multi: Trigger to 1st sample delay	fix	Connector	3 mm SMB male
Multi: Recovery time	< 20 samples	Input impedance	50 Ohm / 1 MOhm 25 pF
ext. Trigger accuracy	1 Samples	Overvoltage protection (range ≤ ±1 V)	±5 V
int. Trigger accuracy	1 Sample	Overvoltage protection (range > ±1 V)	±50 V
Ext. clock: delay to internal clock	42 ns ±2 ns	Warm up time	10 minutes
input signal with 50 ohm termination	max 5 V rms	Operating temperature	0°C - 50°C
Digital Inputs input impedance	110 Ohm @ 2.5 V	Storage temperature	-10°C - 70°C
Digital Inputs delay to analog sample	-4 samples	Humidity	10% to 90%
Min internal clock	1 kS/s	Power consumption 5 V @ full speed	max. 2.3 A (11.5 Watt)
Min external clock	1 kS/s	Power consumption 5 V @ power down	max. 1.9 A (9.5 Watt)
Trigger input: Standard TTL level	Low: -0.5 V > level < 0.8 V High: 2.0 V > level < 5.5 V Trigger pulse must be valid ≥ 2 clock periods.	Clock input: Standard TTL level	Low: -0.5 V > level < 0.8 V High: 2.0 V > level < 5.5 V Rising edge. Duty cycle: 50% ± 5%
Trigger output	Standard TTL, capable of driving 50 Ohm. Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA) One positive edge after the first internal trigger	Clock output	Standard TTL, capable of driving 50 Ohm Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA)

Input range	±50 mV	±100 mV	±200 mV	±500 mV	±1 V	±2 V	±5 V	±10 V
Software programmable offset	±50 mV	±100 mV	±200 mV	±500 mV	±1 V	±2 V	±5 V	±10 V
Offset error	< 1 LSB, adjustable by user							
Gain error	< 1 %	< 1 %	< 1 %	< 1 %	< 1 %	< 1 %	< 1 %	< 1 %
Noise (rms): 50 Ohm, 25 MS/s	< 1.5 LSB	< 1.2 LSB	< 1.0 LSB	< 1.0 LSB	< 1.0 LSB	< 1.0 LSB	< 1.0 LSB	< 1.0 LSB
Crosstalk 500 kHz signal, ±50 mV input, 50 Ohm	< -70 dB							

	MX.3110 MX.3111	MX.3120 MX.3121	MX.3130 MX.3131
max internal clock	1 MS/s	10 MS/s	25 MS/s
max external clock	1 MS/s	10 MS/s	25 MS/s
-3 dB bandwidth	> 500 kHz	> 5 MHz	> 12.5 MHz

Dynamic Parameters

	MX.3110 MX.3111	MX.3120 MX.3121	MX.3130 MX.3131
Test - Samplerate	1 MS/s	10 MS/s	25 MS/s
Testsignal frequency	90 kHz	1 MHz	1 MHz
SNR (typ)	> 67.5 dB	> 64.9 dB	> 63.1 dB
THD (typ)	< -62.8 dB	< -62.5 dB	< -62.5 dB
SFDR (typ), incl harm.	> 80.8 dB	> 80.5 dB	> 79.5 dB
SINAD (typ)	> 61.5 dB	> 60.5 dB	> 59.8 dB
ENOB (based on SINAD)	> 9.9 LSB	> 9.8 LSB	> 9.6 LSB

Dynamic parameters are measured at ± 1 V input range (if no other range is stated) and 50 Ohm termination with the samplerate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave of the specified frequency with > 99% amplitude. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits. For a detailed description please see application note 002.

Order information

Order No	Description	Order No	Description
MX3110	MX.3110 with 8 MSample memory and drivers/SBench 5.x	MX3xxx-16M	Option: 16 MSample memory instead of 8 MSample standard mem
MX3111	MX.3111 with 8 MSample memory and drivers/SBench 5.x	MX3xxx-32M	Option: 32 MSample memory instead of 8 MSample standard mem
MX3120	MX.3120 with 8 MSample memory and drivers/SBench 5.x	MX3xxx-64M	Option: 64 MSample memory instead of 8 MSample standard mem
MX3121	MX.3121 with 8 MSample memory and drivers/SBench 5.x	MX3xxx-up	Additional handling costs for later memory upgrade
MX3130	MX.3130 with 8 MSample memory and drivers/SBench 5.x	MX31xx-dl	DASYLab driver for MX.31xx series
MX3131	MX.3131 with 8 MSample memory and drivers/SBench 5.x	MX31xx-hp	VEE driver for MX.31xx series
MX3xxx-mr	Option Multiple Recording: Memory segmentation	MX31xx-lv	LabVIEW driver for MX.31xx series
MX3xxx-gs	Option Gated Sampling: Gate signal controls acquisition	MATLAB	MATLAB driver for all MI.xxxx, MC.xxxx and MX.xxxx series.
MX3xxx-dig	Additional 4 synchronous digital inputs per channel, incl. cable		
Cab-3f-9m-80	Adapter cable: SMB female to BNC male 80 cm	Cab-3f-9f-80	Adapter cable: SMB female to BNC female 80 cm
Cab-3f-9m-200	Adapter cable: SMB female to BNC male 200 cm	Cab-3f-9f-200	Adapter cable: SMB female to BNC female 200 cm

technical changes and printing errors possible